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2D ferroelectric materials: Emerging paradigms for next-generation ferroelectronics

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ABSTRACT

Ferroelectric materials with electrically switchable spontaneous polarization are technologically important for developing next-generation low-power nanoelectronics and ferroelectronics. Regardless of significant challenges for rich functionalities owing to the insulating nature of conventional thin-film ferroelectrics, ferroelectricity instability or disappearance below a critical thickness limit generally exists. Therefore, exploring emerging two-dimensional (2D) ferroelectric materials with nanoscale dimensions and moderate bandgaps is crucial for developing high-integration functional nanoelectronics. This review offers a comprehensive analysis of the historical background and progression in both thin-film ferroelectrics and novel 2D ferroelectrics. Special attention is given to the device applications based on the emerging 2D ferroelectrics, in which the polarization switching process occurs within the channel material itself. Leveraging the switchable polarization in nanoscale 2D ferroelectrics, rationally designed device configurations with intriguing working mechanisms have been rapidly developed in various application scenarios, such as gate-tunable memristors, non-volatile memories, biological synapses, in-memory computing, etc. This review also sheds light on the potential opportunities and challenges in the future advancement of integrating novel 2D ferroelectric materials into devices within commercial electronic circuits.

Introduction

Ferroelectric materials are functional materials that exhibit stable and switchable spontaneous polarization, which can be reversed by an external electric field. These materials hold great technological significance for multifaceted applications, e.g., memristors, non-volatile memories, logic, artificial intelligence, in-memory computing, etc. (Fig. 1). The initial discovery of ferroelectricity dates back to 1920, which is observed by Valasek in bulk Rochelle salt.[1] Ginzburg et al. developed the first phenomenological theory of ferroelectricity based on Landau's theory of second-order phase transitions in the 1940s, marking a significant advancement in understanding this property.[2] In the 1950s, ferroelectric thin films of perovskite structures were first deposited.[3] Upon successful integration with semiconductors, thin-film ferroelectrics have played a crucial component in electronics and micro-transducers, although a plethora of ferroelectric applications, e.g., memories, low loss power transistors, actuators, etc., mostly used film thickness ranging from 100 nm to several micrometers. Based on the transverse Ising model[4], the size effect in ferroelectric films was analyzed. As the film thickness scales down to below a critical value of several to tens of nanometers, the spontaneous polarization of ferroelectric thin films, e.g., poly(vinylidene fluoridetrifluoroethylene) (P(VDFTrFE)),[5,6] perovskite-type ferroelectrics,[7,8] etc., generally suffers from ferroelectric instability or disappearance.[9] The spontaneous polarization for traditional perovskite oxide in nanoscale is believed to be significantly suppressed by the depolarization field, primarily due to incomplete screening of the polarization-bound charges, surface reconstruction effects, and a decrease in long-range Coulombic interactions.[8,10,11] Simultaneously, the rapid advancement of microelectronics necessitates the production of higher-density electronic

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devices with low-power consumption, leading to a continued trend of shrinking the feature size of materials. Considering the unprecedented challenges posed by the dilemma, significant efforts have been made through surface construction.[12] However, sustaining the ferroelectric polarization until even several unit cells is still challenging, merely through the utilization of selective electrodes and substrates, fabrication of high-crystalline thin films, or other constructive methodologies.[13,14] In this regard, developing controllable thinner ferroelectric materials is crucial for comprehending the size effect and their electronic applications in a post-Moore era.[15]

The advent of atomically thin two-dimensional (2D) layered materials has opened a promising avenue for integrating next-generation nanoelectronic components with nanoscale dimensions and low-power consumption.[16] Essentially, 2D materials are made up of one or a few atomic layers,[17] which make them ideal for sustaining ferroelectric polarization, mainly due to their unique properties, e.g., durability against tremendous strain, dangling bonds, surface states, etc.[18] Since the discovery of graphene exfoliated by Novoselov et al. in 2004, enormous 2D materials, e.g., transition metal dichalcogenides (TMDs), hexagonal boron nitride, MXenes, carbon nitrides, etc., have been revealed.[19] Due to the reduced dimensions compared to their bulk counterparts, 2D materials with strong intralayer chemical bonds but weak interlayer interactions might exhibit reduced symmetry to acquire low-dimensional ferroelectricity.[20] In contrast, 2D layered ferroelectric materials exhibit greater advantages in sustaining ferroelectric polarization owing to their basic properties such as dangling-bond-free surface and outstanding endurance against strain.[21] The microscopic mechanism of 2D ferroelectrics can be more complex, since 2D materials, with multiple stable states and corresponding minimal local energy, could in principle possess ferroelectricity.[9,12] It is because, due to the ultrathin 2D material properties, certain 2D materials are susceptible to the influence of the surrounding environments, leading to extrinsic ferroelectricity through the defect, strain, or surface engineering.[22] Recent theoretical investigations have effectively predicted the intrinsic ferroelectricity of a list of candidates, e.g., 1T-MoS_2,[23–25] In_2Se_3,[26–28] $CuInP_2S_6$,[29,30] and MX (where M = Ge, Sn, and X = S, Se, Te),[31,32] etc. Notably, theoretical calculations of Curie temperatures have indicated that $CuInP_2S_6$ and MX exhibit stable ferroelectricity at room temperature.[33] Therefore, it is expected that the realization of 2D ferroelectricity would facilitate the combination of 2D ferroelectric materials with semiconductor wafers, thereby promoting their prosperous evolution in functional electronics.

Although the study of 2D ferroelectrics is experiencing a notable increase, current research interest in novel 2D ferroelectrics is still in its preliminary stages.[34] It is imperative to emphasize the significant advancements in this burgeoning field, especially on device-level design strategies, operational mechanisms, and advanced device applications. A systematic review on this topic, however, has not yet appeared. In this review, to fully understand the potential and limitations of 2D ferroelectrics, we start with a comprehensive perspective on the historical progression and advancements in the field of ferroelectricity in both thin-film ferroelectrics and novel 2D ferroelectrics, with a particular emphasis on ferroelectric-integrated 2D devices. The rationally designed device structure and underlying operation mechanism are further highlighted. Typical ferroelectric-based 2D devices in various application scenarios are subsequently discussed, e.g., gate-tunable memristor, non-volatile memory, biological synapse, in-memory computing, etc. Lastly, this review extensively discusses the potential opportunities and challenges for the future development of ferroelectric-2D devices, providing a global understanding of prospects and obstacles related to the advancement of such devices.

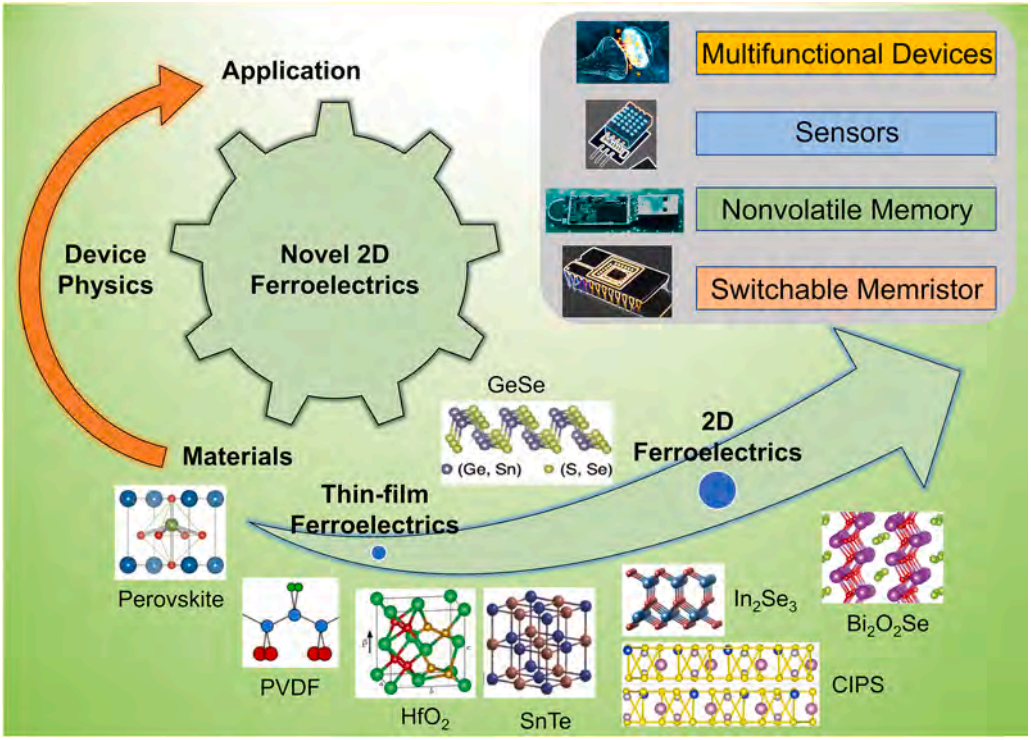


Fig. 1. Development and progress of 2D ferroelectric materials: material structures, device physics and advanced applications in functional electronics. Reproduced with permission for the above crystal structures: Perovskite,[35] Copyright 2013, American Chemical Society., PVDF,[36] Copyright 2019, Elsevier., HfO_2,[37] Copyright 2022, Springer Nature., SnTe,[38] Copyright 2016, American Association for the Advancement of Science., GeSe,[39] Copyright 2022, American Chemical Society., In_2Se_3,[40] Copyright 2016, John Wiley and Sons., CIPS,[30] Copyright 2016, Springer Nature., Bi_2O_2Se,[41] Copyright 2023, John Wiley and Sons., respectively.

Structures and properties of ferroelectrics

To properly comprehend the possibilities and restrictions of 2D ferroelectrics, a complete overview of the historical development and developments in the field of ferroelectricity is required to be particularly stressed in both thin-film ferroelectrics and novel 2D ferroelectrics. Thus, before introducing the device level implementation of 2D ferroelectrics, the typical crystal structures and underlying mechanism of ferroelectricity origin are introduced. Fig. 2a shows the polarization (P)-electric field (E) hysteresis loops, an essential feature of ferroelectric materials. The orientation of the electric dipole moment is initially random, corresponding to point O in the P-E hysteresis loop. The existence of an external electric field could cause alignment of the electric dipole moment with the field direction, resulting in the formation of a polarization field within the ferroelectric material (OA segment). Ferroelectric hysteresis involves the orientation of electric polarization in response to an external electric field, followed by a reversal of polarization upon the reverse of the electric field. Due to a lag between the change in the electric field and the variation of polarization, a ferroelectric hysteresis loop is formed. The P-E hysteresis loop enables the extraction of characteristic parameters that characterize ferroelectrics, such as remnant polarization (Pr) and coercive electric field (Ec), which are believed to determine memory devices' operational voltage and memory window.[42] The structures and properties of distinct types of ferroelectrics will be elaborated, particularly for those experimentally-verified 2D ferroelectric materials. The summary of the

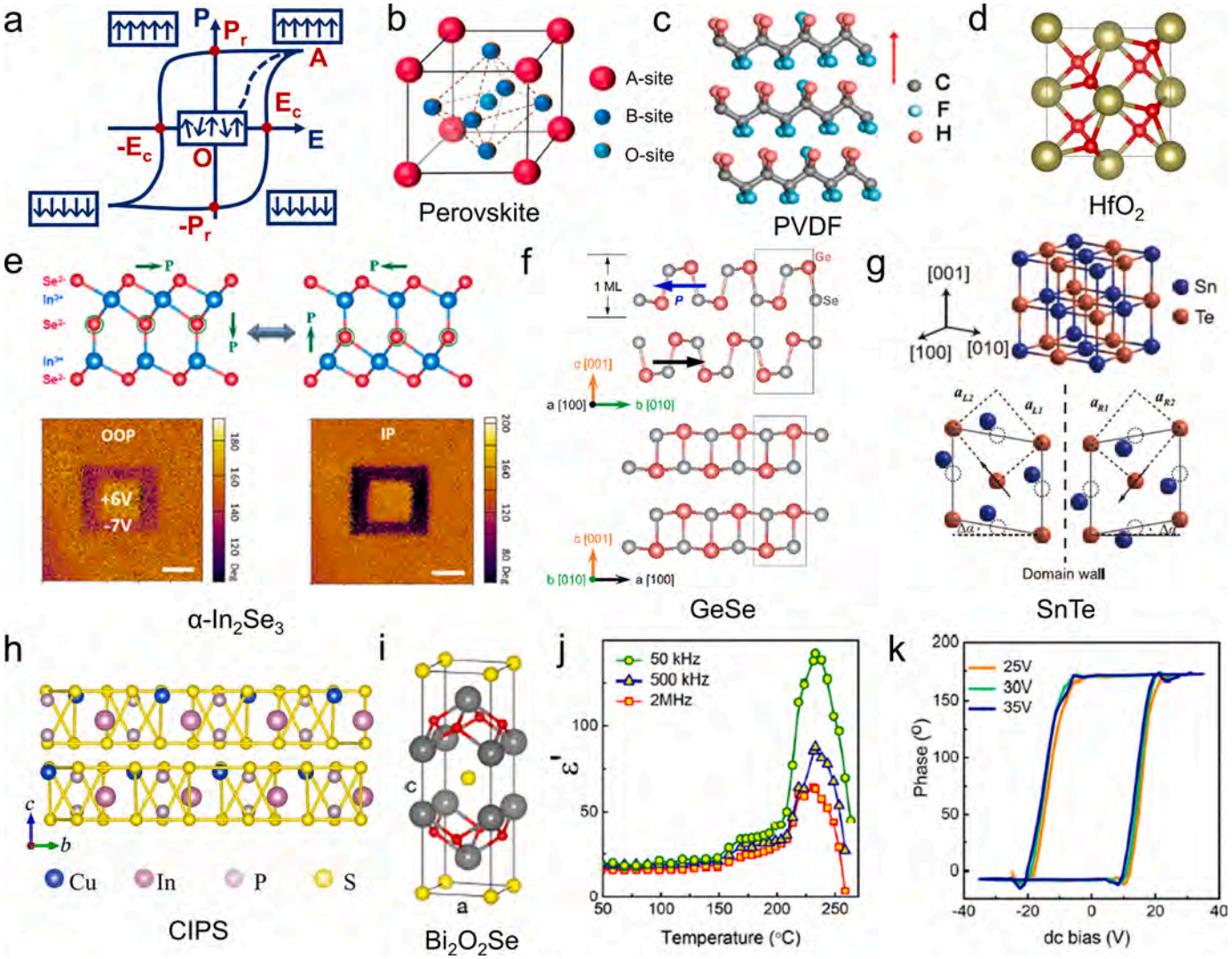


Fig. 2. a) Polarization (P)-electric field (E) hysteresis loops of ferroelectric materials, where Pr and Ec represent the remanent polarization and coercive field, respectively. b) Crystal structures of the ABO_3 type perovskites, where the A and B sites are typically referred to as rare-earth and transition elements, respectively. Both the A and B sites can be replaced by other metal ions. Reproduced with permission.[43] Copyright 2022, American Chemical Society. c) Schematic crystal structure of the P(VDF-TrFE) with the polarization direction indicated by the red arrow. Reproduced with permission.[44] Copyright 2015, John Wiley and Sons. d) Schematic of HfO_2 crystal for the ferroelectric orthorhombic structure ($Pca2_1$). Reproduced with permission.[45] Copyright 2019, AIP Publishing. e) Schematic of the interlocked IP and OOP ferroelectric polarization switching of In_2Se_3 flakes (6 nm) and corresponding OOP and IP phase images with a scale bar of 1 μm after writing two square patterns, respectively. Reproduced with permission.[46] Copyright 2018, American Chemical Society. f) Orthorhombic GeSe crystal structure with two neighboring monolayers (Unit cell). Reproduced with permission.[39] Copyright 2022, American Chemical Society. g) Schematics of the SnTe crystal structure (upper) and ferroelectric-phase lattice distortion (lower). Reproduced with permission.[38] Copyright 2016, American Association for the Advancement of Science. h) Side view of the CIPS crystal structure. Reproduced with permission.[47] Copyright 2016, Springer Nature. i) Tetragonal structure of conventional unit-cell Bi_2O_2Se. Reproduced with permission.[48] Copyright 2022, American Chemical Society. j) Relative permittivity (ε') at distinct frequencies for Bi_2O_2Se ultrathin flakes. k) "Off-field" phase of SS-PFM signal exhibiting a 180° ferroelectric polarization switching at room temperature. j-k) Reproduced with permission.[49] Copyright 2019, American Chemical Society.

properties of representative thin films and 2D vdW ferroelectric materials are compiled in Table 1.

Thin-Film Ferroelectric Materials. In most traditional thin-film ferroelectric materials, e.g., ABO_3-type perovskites, organic polymers like PVDF, doped binary oxide HfO_2, etc., the crystal structures are generally noncentrosymmetric and ferroelectric switching is accompanied by shifting the ions to opposite sides of the cell center.[50] For example, in ABO_3-type ferroelectric perovskite materials (Fig. 2b), where A is Pb^{2+}, Ba^{2+}, etc. and B is Ti^{4+}, Zr^{4+}, etc., the spontaneous polarization generally results from the off-centered ion (B^{4+}) with regards to either upper or lower O^{2-} ions,[51] which has been phenomenologically observed by transmission electron microscope characterization.[14] The intrinsic polarization arises from the cooperative interplay between the short-range electron-repulsive forces that facilitate the development of paraelectric ordering and the long-range Coulomb coupling that stabilizes the ferroelectric ordering.[52] Organic ferroelectrics, such as PVDF, have been extensively studied owing to their cost-effectiveness and remarkable mechanical flexibility. As shown in Fig. 2c, the C–F and C–H bonds in PVDF will generate electric dipoles since the higher electronegativity of the F atom causes the electron cloud to shift towards its side, creating a higher density of negative charges compared to the H side.[53,54] Besides perovskite-type and organic ferroelectrics, room-temperature ferroelectricity in doped binary HfO_2 (Fig. 2d) has been discovered since 2011.[55] The extensive utilization of HfO_2 as a standard dielectric in complementary metal-oxide-semiconductor transistor (CMOS) processes enables its easy integration with current silicon-based semiconductor techniques, whose ferroelectricity in the stable orthorhombic phase is achieved by doping chemical dopants like Zr.[56,57] The polarization of HfO_2 originates from the displacement of four threefold-coordinated O^{2-} ions among the total of eight O^{2-} ions (consisting of 4 threefold- and 4 fourfold-coordinated) within 8 tetrahedral sites surrounded by Hf^{4+} ions.[58] In this section, our intention is not to provide a detailed review on conventional thin-film ferroelectric materials, but rather to formulate a framework on related classic ferroelectric mechanism, which could help us understand the appearance of the novel 2D ferroelectrics.

Table 1
Summary of the properties of representative thin films and 2D vdW ferroelectric materials.

Material (Ref.)	Space/ point group	P (μC cm^{-2})	E_c (kV cm^{-1})	T_c (K)	Bandgap (eV)
AlScN[73]	—	25	6500	20 nm, above RT	—
P(VDF-TrFE)[74]	—	7	750	300 nm, 400 K	7.7eV
HfO_2[75]	$P2_1/C$	10	1000	10 nm, above RT	—
$CuInP_2S_6$[76]	Cc	2.55	77	5 ML, >320	Bulk, 2.7
1T'-ReS2[77]	C_i	0.07–0.68 pC m^{-1}	—	≥2 ML-7ML, 450	—
SnTe[38]	$Pnm2_1$	1 ML, 22^T	—	1 ML, 270; bulk, 100	1 ML, 1.6; bulk: 0.3
SnSe[78]	$Pnm2_1$	—	1 ML, 140	1 ML, >380	1 ML, 2.1; bulk: 0.9
SnS[78]	$Pnm2_1$	—	9 ML, 25; bulk, 10.7	1 ML, >300	1 ML, 1.6; bulk: 1.2
GeTe[79]	R3m	1 ML, 32.8	~0.2 V nm^{-1}	1 ML, 570T	Bulk, 0.6
γ-InSe[80]	3/mmc	—	—	≥2 ML, >300	Bulk, ~1.4
α-In_2Se_3[81]	R3m	Bulk, 11.34^T; 1 ML, 2.14^T	5 nm: 200	4 ML, 700	1 ML, 2.8; bulk, 1.45
d1T-$MoTe_2$[82]	d-P3m	—	—	1 ML, 330	2–3 ML, 0; bulk, 0
Td-WTe_2[83]	$Pnm2_1$	0.2 pC m^{-1}	0.05 V nm^{-1}	2–3 ML, 350	2–3 ML, 0; bulk, 0
WSe_2, $MoSe_2$, WS_2, MoS_2[84,85]	—	~2.0 pC m^{-1}	~0.2 V nm^{-1}	2 ML, >300	—
Heterobilayer MoS_2/WS_2[86]	3m	1.45 pC m^{-1}	2.4 V nm^{-1}	2 ML, >300	2 ML, >300
Twisted bilayer h-BN[22,87]	—	~1.88 pC m^{-1}	~0.1 V nm^{-1}	2 ML, >300	2 ML, >300
Twisted bilayer graphene/h-BN [88]	—	~0.09	~0.2 V nm^{-1}	2 ML, >300	—
BA_2PbCl_4[89]	$Cmc2_1$	13	50 nm, 350	2 ML, >300	Bulk, 3.65
NiI_2[90,91]	d-R3m	0.0125	—	Bulk, 59.5; 1 ML, 21	Bulk, 1.2
Bi_2O_2Te[92]	I4/ mmm	—	—	2 ML,	Bulk, ~0.15 eV
Bi_2O_2Se[69]	d-I4/ mmm	56.1	—	≥2 ML, 455	2–3 ML, Bulk, 0.8

P, polarization; E_C, coercive field; T, theoretical calculation; ML, monolayer; —, unconfirmed; d, distorted.

Novel 2D Ferroelectrics. Despite theoretical predictions of 2D ferroelectricity in a broad selection of 2D layered materials, merely a limited number of 2D ferroelectric materials have been experimentally realized and investigated thus far, e.g., α-In_2Se_3,[27,28,59–61] GeSe, [62,63] SnTe,[64–66] CIPS,[47,67,68] Bi_2O_2Se[41,48,49,69], etc. Li et al. experimentally observe the robust intralayer room-temperature ferroelectricity in ultrathin α-In_2Se_3 flakes.[70] The polarization process was investigated by transferring α-In_2Se_3 flakes onto a Si substrate coated with Au (or Pt). In_2Se_3 displays intrinsic intercorrelated polarization reversal in the out-of-plane (OOP) and in-plane (IP) directions, where the OOP polarization reversal simultaneously triggers a related IP polarization reversal and vice versa. Theoretical calculations have demonstrated the inherent origin of the unique IP and OOP intercorrelation, which can be attributed to the electric field-induced lateral movement of the central Se atomic layer in the FE-ZB′ configuration (Fig. 2e). The corresponding OOP and IP phase image of 6-nm-thick In_2Se_3 flake after writing two square zones with opposite tip voltages (+6 and −7 V) by piezoelectric force microscopy (PFM), indicating the excellent stability and controllability of the written domains under the external bias. It is worth pointing out that the coexisting of OOP and IP polarization components in In_2Se_3 remains controversial since the locking between OOP dipoles and IP lattice is asymmetric.[71] It is because the in-plane dipole shown in Fig. 2e can be canceled by in-plane 3-fold rotation symmetry, just like the case of monolayer MoS_2 with broken inversion symmetry but without IP net polarization. Given that there is no net IP polarization component in In_2Se_3, the IP PFM signal in Fig. 2e could be a crosstalk artifact between the OP and IP signals.

Duan et al. made an experimental discovery of the electric-field-induced transition from antiferroelectric (AFE) to ferroelectric (FE) in α-GeSe flakes, which was corroborated by various techniques, including transmission electron microscopy (TEM), PFM, second-harmonic generation (SHG), and first-principles calculations, etc.[39] Temperature-dependent Raman spectra demonstrate strong evidence of in-plane (IP) polarization up to 700 K along the armchair direction, as opposed to the zigzag direction (Fig. 2f). The stable IP ferroelectric polarization of 1-unit-cell-thick SnTe flakes is unrevealed since the formation of the ferroelectric domains is observed with parallel stripes along the [010] direction.[38] The ferroelectric origin of the atomically thin SnTe is comprehensively investigated, which can be derived from the lattice distortion and Sn displacement in the rock-salt structure (Fig. 2g). Fig. 2i illustrates the tetragonal anti-$ThCr_2Si_2$ structure of

Bi_2O_2Se flakes which have an I4/mmm space group symmetry ($a = 3.89$ Å, $c = 12.21$ Å).[48] Here, the bulk Bi_2O_2Se crystal structure is centrosymmetric, in which each Se atom is situated in the cubic center of the eight Bi atoms. Given the centrosymmetric crystal structure in the bulk phase, the room-temperature ferroelectricity of ultrathin Bi_2O_2Se nanoflakes is quite surprising.[49] Combing the temperature-independent dielectric characteristics at distinct frequencies (Fig. 2j) with differential scanning calorimetric (DSC) signal, the ferroelectric transition is observed, demonstrating the existence of the spontaneous polarization state in ultrathin Bi_2O_2Se nanoflakes.[49] To further confirm the ferroelectric switching property, the "off-state" hysteric loops by the PFM test are observed with a sharp 180° ferroelectric reversal at distinct dc bias (Fig. 2k). The ferroelectric order in ultrathin Bi_2O_2Se flakes at room temperature can be attributed to spontaneous orthorhombic distortion induced by atomic displacements of Bi and O atoms,[41,49] even without considering the factors, e.g., surface effects, strain,[48,69,72] doping, etc. The emerging room-temperature ferroelectric 2D materials hold great significance as they open up new possibilities for developing diverse applications in non-volatile memories, sensors, electronics, and other fields.

Device physics of emerging 2D ferroelectrics

In order to achieve diverse functionality for next-generation electronics, 2D ferroelectrics must be integrated into different architectures,[93] such as ferroelectric tunnel junction,[94] ferroelectric diode,[95] etc. This review pays special attention to ferroelectric-based field-effect transistors (FETs) owing to their prominent and wide utilizations in the era of modern semiconductor technology. Semiconductor devices using electric field effects to control their output characteristics are classified as field-effect transistors (FETs), unipolar transistors due to their reliance solely on majority carriers for operation. The conventional ferroelectric field-effect transistor (FeFET) was conceptualized in the 1950s,[96,97] in which a ferroelectric layer serves as the gate insulator in a standard metal-oxide-semiconductor field-effect transistor (MOSFET). To date, the FeFETs, potentially working as a non-volatile memory element, continue to be a commercially infeasible technology [98] due to interfacial issues such as depolarization and poor channel controllability.[99] Emerging 2D ferroelectrics, owing to their dangling-bonds-free surface, provide new opportunities for conventional FeFETs to mitigate interfacial charge trapping and current leakage.[100] The performance degradation caused by interfacial issues in conventional ferroelectric FeFETs can be effectively mitigated using 2D ferroelectrics as gate insulators or channel semiconductor layers. For instance, integrating 2D ferroelectric insulators with 2D semiconductors holds promise in mitigating depolarization field and current leakage issues in conventional FeFETs.[100–102] In addition to conventional FeFETs that necessitate a high-quality polycrystalline ferroelectric insulator, new device structures related to 2D ferroelectric semiconductors, ferroelectric semiconductor FETs (FeSFETs), are recently developed with better compatibility of amorphous gate insulators.[100] The working principle of FeSFETs differs from that of conventional

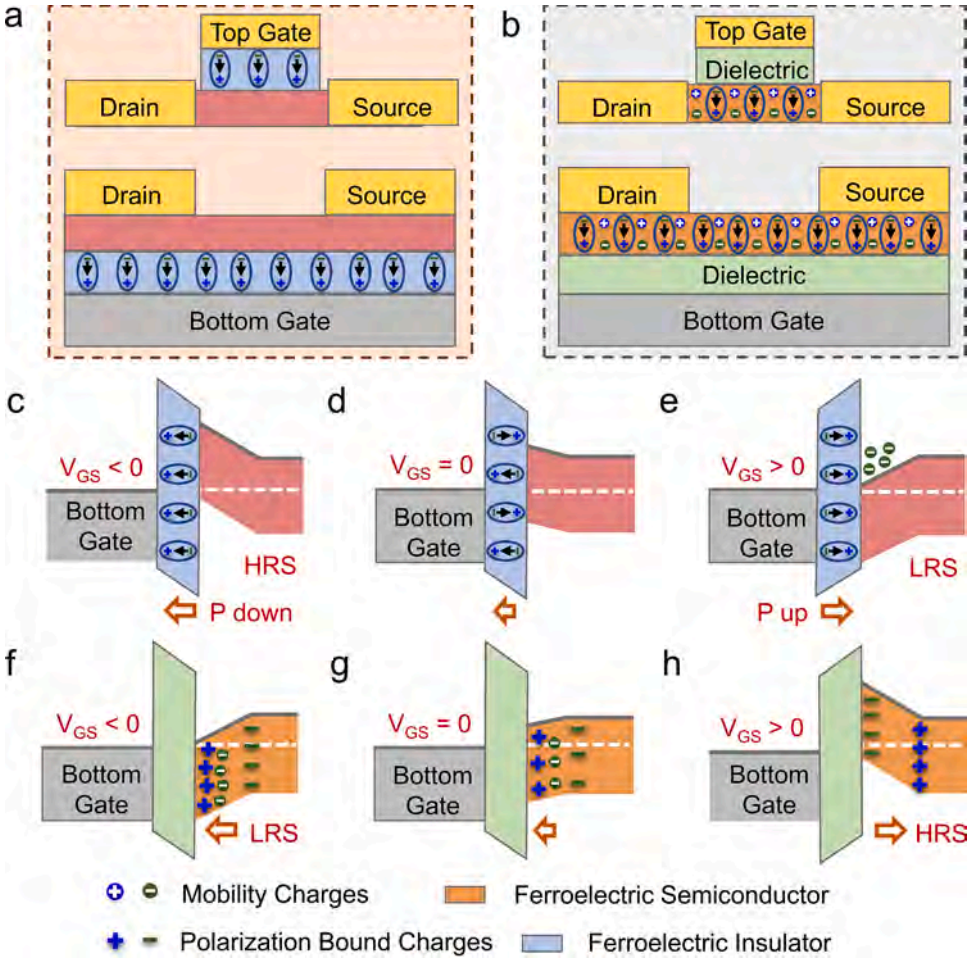


Fig. 3. a-b) Schematics of the typical top-gated (upper) and bottom-gated (lower) device configurations for FeFETs utilizing 2D ferroelectrics as insulator layers (a) and FeSFETs using 2D ferroelectric semiconductor as channel layers (b). c-e) Schematic band diagrams of the bottom-gated FeFETs as the gate voltage sweeps from a negative (c), zero (d), and finally to a positive bias (e), respectively. f-h) Schematic band diagrams of the bottom-gated FeSFETs as the gate voltage sweeps from a negative (c), zero (d), and finally to a positive bias (e).

FeFETs. Therefore, it is crucial to provide an overall comparison between traditional FeFETs and FeSFETs on their device architectures and associated physics in order to better comprehend the possible uses of 2D ferroelectric materials.

Ferroelectric field-effect transistors (FeFETs)

Fig. 3a illustrates the device structures of typical top-gated (upper) and bottom-gated (lower) FeFETs that employ 2D ferroelectrics as insulator layers. For simplicity, only the mechanism of channel formation in bottom-gated FeFETs with an n-type semiconductor is demonstrated. Fig. 3c-e shows the energy band bending between the insulator layer and the semiconductor layer as the gate electric field sweeps from the negative ($V_{GS} < 0$) to positive voltages ($V_{GS} > 0$ V). Applying a negative voltage to the gate causes the valence band edge (E_V) to bend above the Fermi level (E_F) of the n-type semiconductor, leading to the generation of holes and the formation of high channel resistance states (HRS) in the semiconductor layer. As the gate voltage sweeps to $V_{GS} = 0$ V, the ferroelectric insulator retains its remanent up-state polarization (Fig. 3d). Conversely, when a high gate voltage capable of inducing polarization switching is applied to the ferroelectric layer, the conduction band edge (E_C) bends below the Fermi level (E_F) of the n-type semiconductor. This phenomenon will induce the generation of mobile electrons, resulting in low channel resistance states (LRS) in the semiconductor channel (Fig. 3e). In the case of the FeFETs, utilizing ferroelectric insulators with a high remnant polarization (Pr) or low coercive field (Ec) offers advantages in driving FeFET devices. This is due to the spontaneous ferroelectric polarization that creates regions of accumulated or depleted carriers within the device structure.[103,104] The ferroelectric polarization switching of the insulator layer (up or down) could either enhance the inversion layer or deplete the semiconductor channel, thus leading to opposite threshold voltage shifts.[105] Therefore, it is possible to vary the channel conductance in FeFETs by changing the ferroelectric polarization state of the gate insulator, exhibiting considerable potential in electronics, e.g., non-destructive, fast-response, and high-integrity memory.[106]

Ferroelectric semiconductor field-effect transistors (FeSFETs)

Leveraging the emerging discovery of 2D ferroelectric semiconductors, e.g., In_2Se_3,[61],$MoTe_2$,[82] SnS,[107] etc., a new device concept called ferroelectric semiconductor FETs (FeSFETs) with distinct working principle was developed. Fig. 3b exhibits the device configurations of the FeSFETs, in which 2D ferroelectric semiconductors could serve as the semiconductor layer instead of the insulator layer, providing a new material platform for the rational design of device structures and high-density integration.[41] In contrast to conventional FeFETs, ferroelectric polarization reversal exists in the 2D ferroelectric semiconductor channel.[100] The mobile charges in the ferroelectric semiconductor can effectively screen the depolarization field across the semiconductor, [41,100] potentially applicable for eliminating the charge trapping and leakage current through the ferroelectric insulator present in conventional FeFETs.[98],[108] This advantage could be attributed to the coupling of the ferroelectricity and semiconducting property in 2D ferroelectric semiconductors,[109] as well as their dangling-bond-free interfaces. In FeSFETs, the channel conductance is synergistically determined by the bottom and top surfaces of the semiconductor. As Fig. 3f ($V_{GS} < 0$) demonstrated, the electron density at the insulator/ferroelectric semiconductor is high in the polarization up state, leading to the LRS. When an enough high positive gate bias is applied, the channel polarization gradually reverses into a polarization down state, depleting electrons and resulting in the high-resistance state (HRS) in the channel layer (Fig. 3g-h). Consequently, FeFETs and FeSFETs exhibit hysteresis loops with different directions (I_{DS} versus V_{GS}) as the gate bias varies from negative to positive voltage.[100,110,111] The channel conductance of hysteretic curves in both FeFETs and FeSFETs can be regulated by the polarization direction, presenting significant potential for functional electronics, e.g., memory, synapse operation, etc. By manipulating the polarization state through gate voltage regulation, it is possible to achieve multi-level channel conductance, thereby enhancing the versatility of these device structures.[102,112]

Fig. 4a showed the side and top view of the α-In_2Se_3 structure under an out-of-plane polarization state,[113] and the ferroelectric hysteresis curves were tested after transferring CVD-grown α-In_2Se_3 flakes onto HOPG substrate (Fig. 4b).[114] Both out-of-plane (OOP) and in-plane (IP) ferroelectric polarization signals of α-In_2Se_3 were detected (Fig. 4c).[59] The conventional butterfly curve and 180° phase change in Fig. 4d demonstrate the ferroelectric polarization flipping of α-In_2Se_3 flakes. Previous research has shown that the stability of α-In_2Se_3 ferroelectricity can be enhanced through the interlocking of OOP and IP polarizations rather than relying solely on conventional long-range Coulomb interactions.[115] The fabrication of FeSFETs involves utilizing the ferroelectric α-In_2Se_3 semiconductor as the channel material due to its favorable properties, such as a moderate bandgap of approximately 1.39 eV,[116,117] atomically-thin ferroelectricity with a high Curie temperature (>200 °C),[118,119] and feasibility for large-area synthesis and integration.[120] Chen et al.[100] developed 2D FeSFETs using α-In_2Se_3 as the channel material and systematically investigated the performance of these devices (Fig. 4e). The operation of FeSFET devices relies heavily on the coupled ferroelectric and semiconducting nature of α-In_2Se_3 nanoflakes.

By its semiconducting characteristics, the channel can exist mobile charges depending on the relative positions of the conduction/valence band edges and the Fermi level (E_F). The existence of the electrons can form a non-uniform distribution of the electric field (E field) across different layers of α-In_2Se_3, with the magnitude of the E field in the channel determining the extent of polarization switching in the α-In_2Se_3 layers. Therefore, owing to the coupled ferroelectric and semiconducting nature, the multi-level channel conductance of hysteretic curves in α-In_2Se_3 FeSFETs can be regulated by the polarization direction itself under different external electric fields. The synergetic interactions in the proposed device result in distinct characteristics, broadly classified as clockwise or counterclockwise hysteresis. The hysteretic direction in the FeSFETs is determined by the E field in the channel due to different effective oxide thicknesses (EOTs): high EOT and low EOT. Clockwise hysteresis curves can be induced for high EOTs with 90 nm SiO_2 (Fig. 4g-h). This can be attributed to the partial polarization of α-In_2Se_3 under a limited electrical field, where the channel conduction depends on the accumulated electrons at the bottom interface. In low-EOT FeSFETs with 15 nm HfO_2, a sufficiently high electric field can fully polarize α- In_2Se_3, and therefore induce the electrons accumulation at the top surface of α-In_2Se_3 channel (Fig. 4i). In the polarization-up state, counterclockwise hysteresis curves can be observed, with a high current on/off ratio of $>10^8$ and maximized on-current intensity of 862 μA μm^{-1} (Fig. 4j). The above discussion regarding the hysteresis behavior is a simplified picture without considering the factors, e.g., interface trapping, intrinsic defects or traps, etc.,[41,121] which generally produce a clockwise hysteresis in most n-type FETs. With their superior performance, huge memory windows, high on/off ratios, and low supply voltage, these FeSFETs, which use 2D ferroelectric semiconductors as channel materials, show significant promise for non-volatile memory applications.

Novel ferroelectric devices

Bistable FeS-PDs

Attributed to the coupling of ferroelectricity with semiconducting characteristics, 2D layered ferroelectric semiconductors theoretically possess prominent switchable features under an external electric field, exhibiting great potential in bistable optoelectronics. Fig. 5a illustrates the synthesis of 2D ultrathin Bi_2O_2Se flakes with a large size of ~100 μm

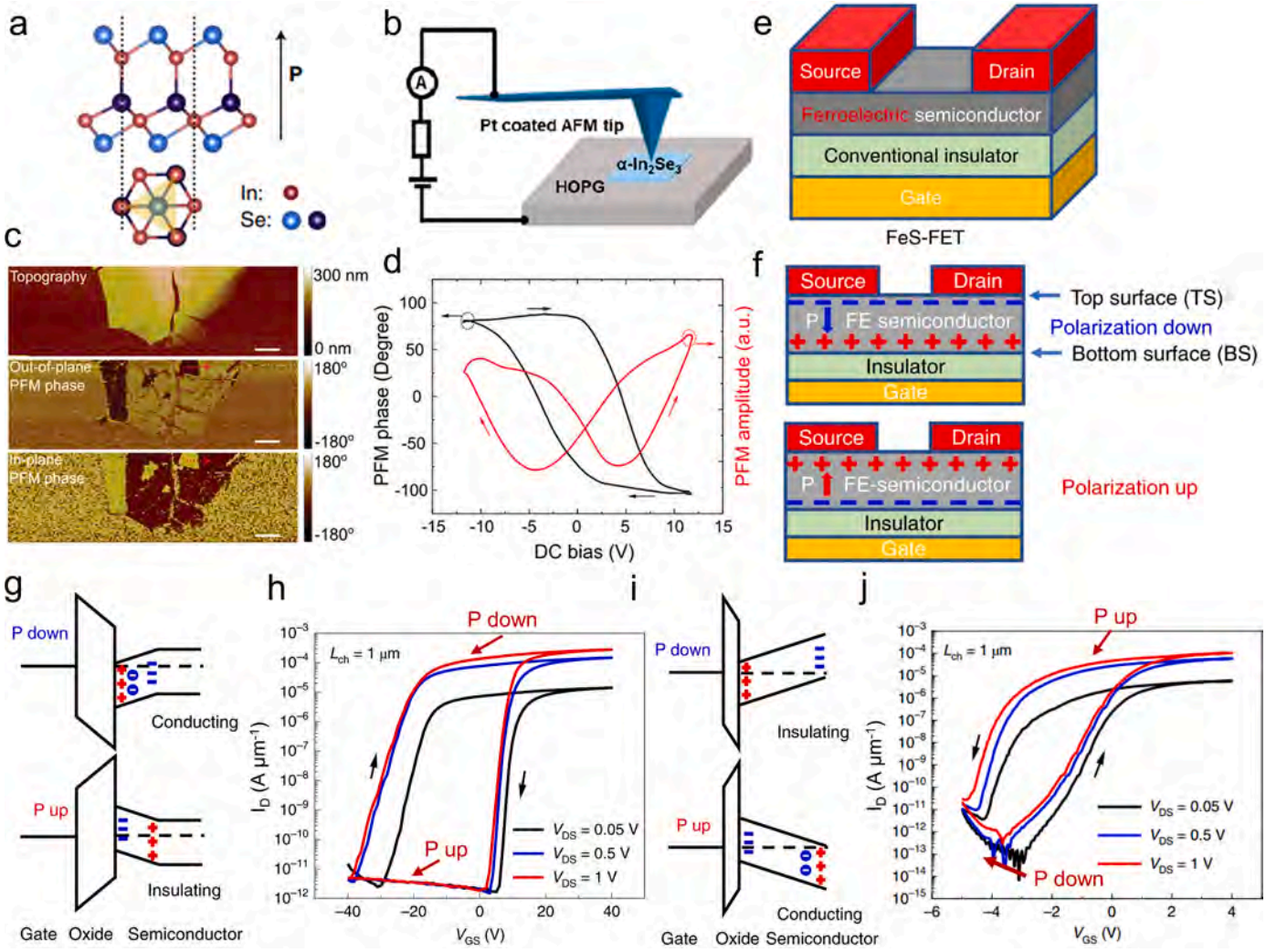


Fig. 4. a) Schematics of side- and top-view of ferroelectric In_2Se_3 with upward OOP ferroelectric polarization. Reproduced with permission.[113] Copyright 2018, American Physical Society. b) Schematic of the PFM test utilizing the Pt/In_2Se_3/HOPG structure. Reproduced with permission.[122] Copyright 2023, American Chemical Society. c) Morphology (Top), OOP PFM phase (middle), and IP phase (bottom) image of In_2Se_3 nanoflakes with opposed ferroelectric polarization. d) Hysteretic characteristics of OOP PFM phase and amplitude under DC tip bias, indicating the ferroelectric polarization reversal. c-d) Reproduced with permission. [59] Copyright 2020, John Wiley and Sons. e) Schematic of the FeSFET with a ferroelectric semiconductor and conventional gate insulator. f) Distribution of the polarization bound charges in FeSFETs in downward states under negative gate bias and upward states under positive gate bias. g-h) Schematic band diagram of FeSFETs under opposite polarization states with high effective oxide thickness (EOT) and clockwise hysteretic transfer curves. i-j) Band diagram of FeSFETs under opposite polarization states with low EOT and counterclockwise hysteretic transfer curves. e-i) Reproduced with permission.[100] Copyright 2019, Springer Nature.

using the chemical vapor deposition (CVD) method.[123] These flakes have been discovered with room-temperature ferroelectricity owing to the inverse symmetry-breaking caused by spontaneous lattice distortion. [49,69] To gain a deeper understanding of the formation of Bi_2O_2Se ferroelectricity, AIMD simulations of local dipoles at finite temperatures were conducted. Fig. 5b illustrates a snapshot from the ground-state MD simulation, depicting fluctuations and random orientations of local dipoles at each instance.[124] The energy barrier that separates the local distorted and pristine lattice is approximately 4.3 meV, which is far below k_BT at room temperature (≈25.9 meV), producing a fluctuating landscape of local dipoles in ultrathin Bi_2O_2Se flakes.[124] The typical "OFF-field" curves of ferroelectrics, featured by a sharp 180° phase reversal with a butterfly-shaped amplitude loop at the coercive voltage (V_{DC} = ±5 V), are well observed in ultrathin Bi_2O_2Se nanosheets (Fig. 5c), using a dual AC resonance tracking PFM technique (DART-PFM, Asylum Research). The technique can eliminate the spurious electrostrictive and electrochemical forces that can otherwise produce ferroelectric-like piezoresponse feedback, recording the remnant piezoresponse signal of the ferroelectric-induced response in CVD-grown Bi_2O_2Se nanosheets.[125,126] Furthermore, density functional theory calculations (DFT) were performed on ultrathin-distorted Bi_2O_2Se with symmetry breaking to uncover the underlying mechanisms of electrically dependent ferroelectricity. Fig. 5d displays the electron density redistribution (Δρ) under the electric field of +0.1 V Å^{-1} and –0.1 V Å^{-1}, respectively. The reverse charge redistribution under the positive and negative electric fields confirms the electrically switchable polarization direction of ultrathin Bi_2O_2Se flakes.

The interplay between ferroelectricity and semiconducting characteristics is explored under distinct electric field relative strength in high EOT/low EOT by introducing a new *x*-axis of V_{GS}/EOT. High-EOT devices exhibit clockwise hysteresis loops (Fig. 5e, upper) due to the interface trapping and intrinsic defects or traps in n-type FETs,[127] caused by the insufficient strength of the electric field. In contrast, low-EOT devices exhibit typical ferroelectric-induced hysteresis with a counterclockwise direction as the V_{GS} sweeps to higher voltages (Fig. 5e, lower). In contrast to the trap-driven clockwise hysteresis, the counterclockwise observation provides conclusive evidence of ferroelectric polarization reversal in 2D Bi_2O_2Se FeSFETs.[100] Following the

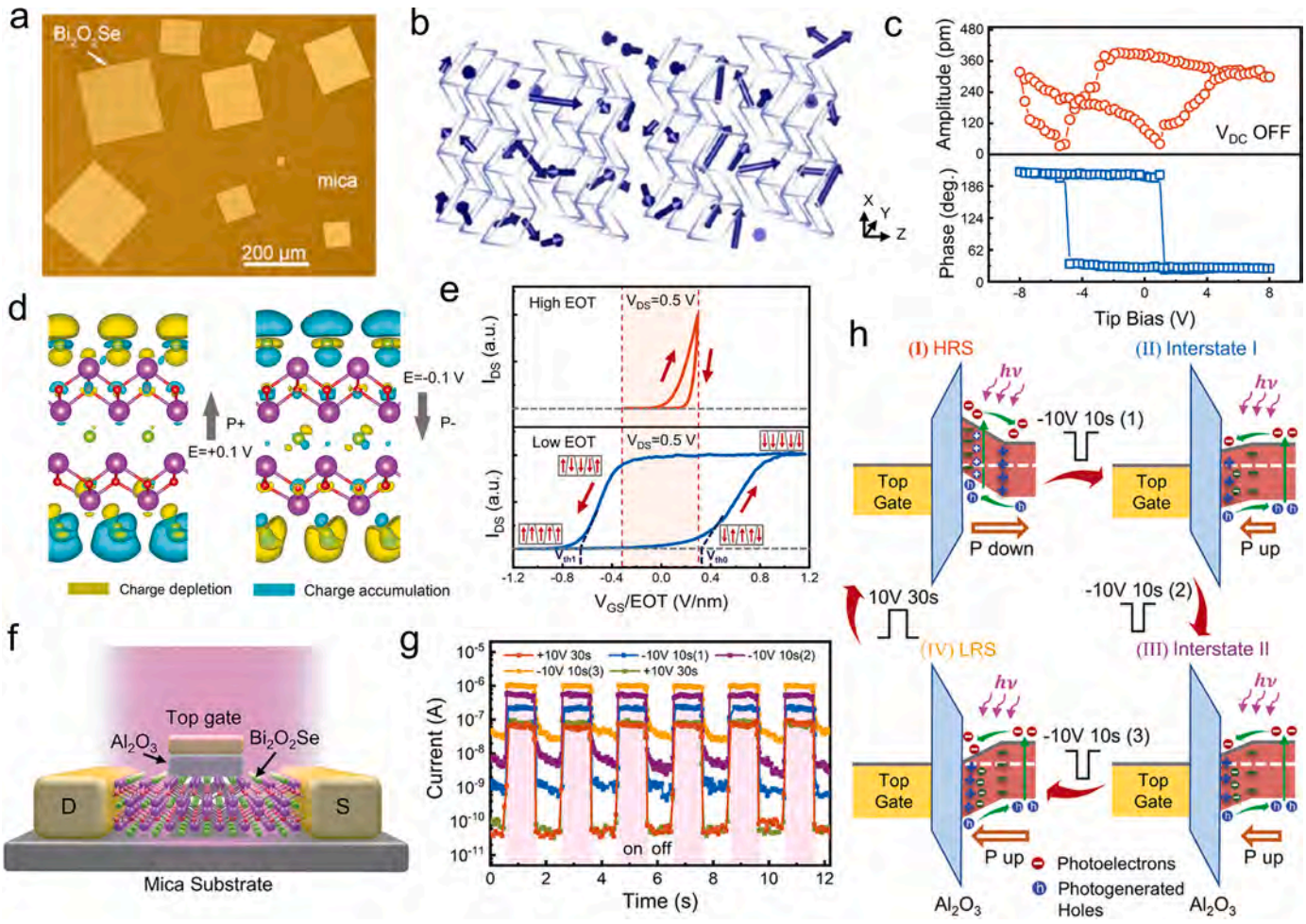


Fig. 5. a) Optical image of CVD-grown single-crystalline 2D Bi_2O_2Se nanosheets on mica substrate with submillimeter sizes. Reproduced with permission.[123] Copyright 2019, American Chemical Society. b) Schematic snapshot of simulated local dipoles via molecular dynamics (MD) techniques, generated by calculating the sum of the product between the displacements and formal charges of Bi/O/Se atoms in a unit cell. Reproduced with permission.[124] Copyright 2022, Proceedings of the National Academy of Sciences. c) "Off-field" amplitude (upper) and phase (lower) hysteretic curves of the 7.3 nm-thick Bi_2O_2Se nanosheets. d) Iso-surface electron density difference ($\Delta\rho = \rho_e - \rho_0$) between with electric fields of ± 0.1 V Å^{-1} (ρ_e) and without electric fields (ρ_0), respectively. e) Contrast the hysteretic behavior for FeSFETs with low EOT (counterclockwise) and high EOT (clockwise) by using the new *x*-axis of V_{GS}/EOT. f-g) Schematic of the FeS-PD device (f) and corresponding photoresponse after withdrawing different gate voltages (g), respectively. h) Schematics of the band diagrams in HRS, Interstate I, Interstate II, and LRS after applying distinct gate voltages and potential separation of the photogenerated electron-hole pairs in ferroelectric semiconductor channel caused by the remanent polarization. c-h) Reproduced with permission.[41] Copyright 2023, John Wiley and Sons.

investigation of the performance of 2D Bi_2O_2Se ferroelectrics in electronics, a ferroelectric semiconductor photodetector (FeS-PD) was fabricated to demonstrate the coupling effect between photoelectricity and ferroelectricity at the device level utilizing 2D Bi_2O_2Se FeSFETs. Fig. 5f depicts the device configuration of the FeS-PD, while Fig. 5g illustrates its relevant optoelectronic response with distinct polarization levels. Under distinct bistable channel conductance corresponding to different channel polarization states, the related gate bias can effectively control both photo- and dark currents. This result is also observed in previously-reported In_2Se_3-based FeS-PD,[128] and can be attributed to electron accumulation in the Bi_2O_2Se channel. Owing to electron accumulation, a built-in electric field that consolidates and reinforces the remnant polarization after each pulse stimulation can be generated.[129,130] Fig. 5h illustrates the band diagrams of the FeS-PD resulting from the remanent polarization and the potential separation of photogenerated electron-hole pairs in a ferroelectric semiconductor channel under 405 nm. The investigation of the FeS-PD lays the foundation for developing 2D ferroelectric-based optoelectronics, exhibiting promising perspectives on bistable FeS-PDs that can be employed in other emerging 2D ferroelectric semiconductors simultaneously.

Gate-Tunable memristor

Memristive devices, proposed as the fourth fundamental circuit element,[131,132] have attracted significant research interest for their potential use, e.g., non-volatile memory, logic, biological synapses, etc. Achieving precise control over the conducting paths resulting from the resistance switching in memristive devices is critical for their performance optimization, particularly regarding ON/OFF ratios. Ferroelectric memristors, commonly maintaining ON/OFF resistance states through the ferroelectric reversal, basically possess high on/off switching ratios, long-term retention, and simple device configurations.[133,134] Thus, ferroelectric memristors exhibit strong appeal for digital data storage and synaptic mimicry, which also meet the demands for high-density memory solutions for artificial intelligence. Despite the potential impact of the ferroelectric memristors, developing multiterminal programmable memristors with optimized output and minimal device-to-device variations is still challenging. The discovery of the 2D ferroelectric semiconductors coexisting electron carriers and switchable polarization in the channel itself provides possibilities for novel ferroelectric memristor that combine the gate and channel layers in one to realize resistance switching, which could enable to create novel device

configurations for multiterminal memristors. α-Ga_2Se_3 is a typical III_2VI_3 native defective compound semiconductor with one-third of the ordered structural vacancies of Ga, which is attributed to the valence mismatch between Ga and Se elements.[135] Fig. 6a demonstrates the polarization reversal in α-Ga_2Se_3 supercell under an appropriate external electric field along the (100) axis, ultimately causing a long-range reversed polarization by moving Ga vacancy between neighboring asymmetrical sites. The clear observation of the butterfly-like amplitude loop and the 180° phase reversal provides additional evidence of OOP ferroelectricity for α-Ga_2Se_3 nanoflakes. To probe the IP polarization switching at the device level, the devices with a channel length of ≈10 μm are fabricated on SiO_2 (285 nm)/Si substrate after transferring the 10 nm thick α-Ga_2Se_3 nanoflake (Fig. 6c). The transfer curve (Fig. 6d) shows that the 2D α-Ga_2Se_3 device exhibits typical p-type conductive characteristics at $V_{ds} = 0.5$ V. The FeFET device displays a switchable diode effect under opposite voltage bias poling (Fig. 6e), resulting from the asymmetric regulation of the Schottky barriers through ferroelectric polarization bounded charges. Under negative bias poling, negative polarization charges will accumulate at the source terminal, reducing the barrier height and increasing the current in the α-Ga_2Se_3. Oppositely, increased Schottky barriers and a decreased current will be produced owing to the accumulation of positive bounded charges at the source terminal under positive bias poling. The observation of the switchable diode effect is consistent with IP polarization in the as-grown α-Ga_2Se_3 nanosheets.

Fig. 6f illustrates that every individual α-In_2Se_3 monolayer consists of five atomic layers bonded by covalent interactions in Se-In-Se-In-Se. The room-temperature ferroelectricity of α-In_2Se_3 with interlinked OOP and IP dipoles could be stabilized down to the monolayer limit owing to its intrinsic asymmetric structure.[61,71] Based on the 2D Ge_2Se_3 ferroelectric semiconductor, Zhang et al. successfully implemented and investigated the gate-tunable programmable memristive devices with a similar structure (Fig. 6c).[136] As demonstrated by the black arrows in Fig. 6g, the two-terminal α-In_2Se_3 memristor initially shows an LRS as the V_{Drain} swept from the negative V_{max} (−6 V) to 0 V (sweep i), followed by a transition to a HRS. The HRS maintains until the V_{Drain} increases to

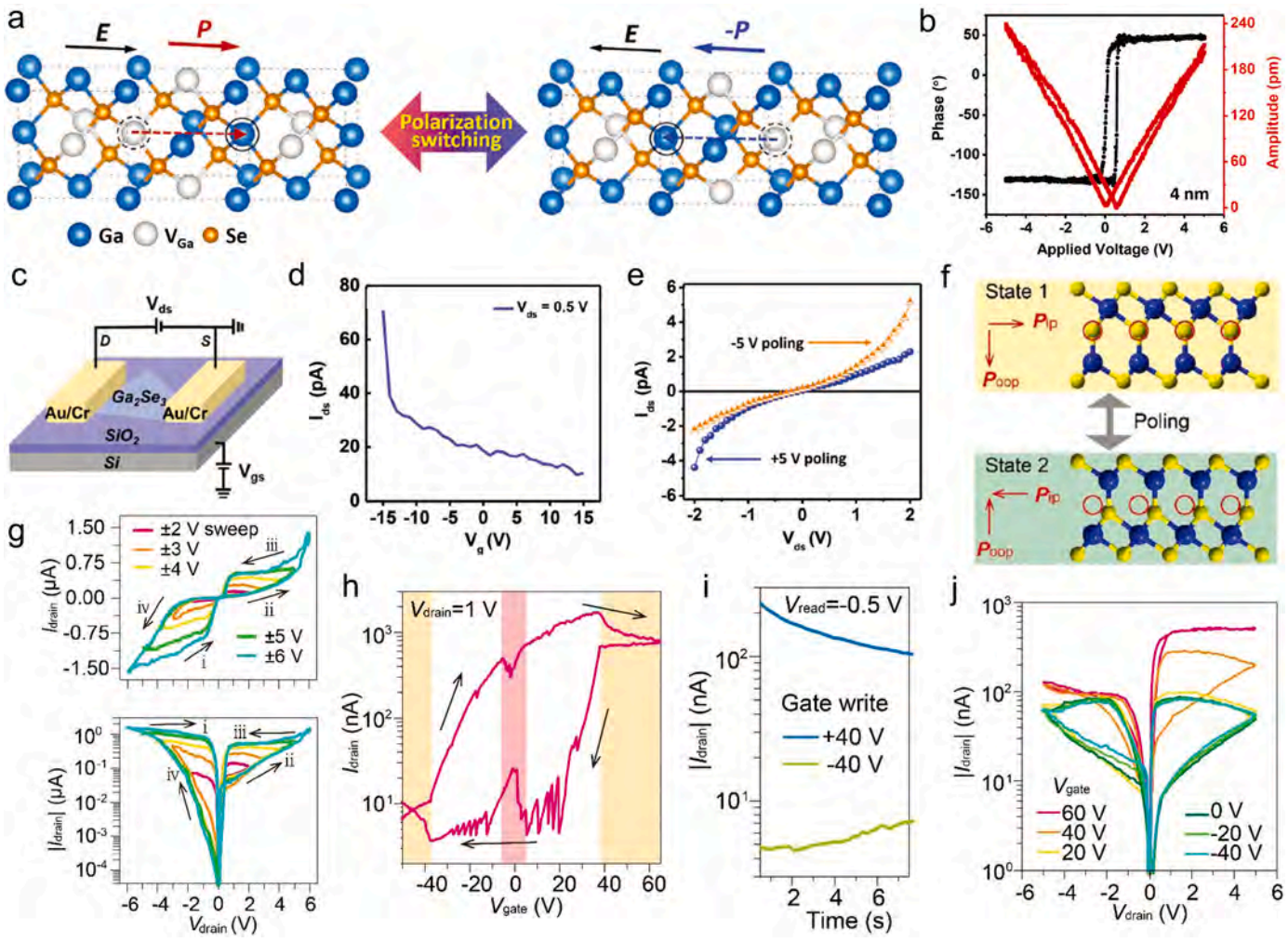


Fig. 6. a) Schematic of the long-range polarization flipping under external electric field along (100) axis by moving Ga vacancy into adjacent asymmetrical sites. b) Hysteretic behavior of amplitude (red) and phase (black) loops for α-Ga_2Se_3 nanoflakes (~4 nm). c) Schematic of the α-Ga_2Se_3 (≈10 nm) based FeFET device to measure the switchable ferroelectric diode effect. d) Typical p-type transfer curves of the device. e) Switchable diode behaviors of the FeFET device under polling voltages of ±5 V, respectively. a-e) Reproduced with permission.[137] Copyright 2022, John Wiley and Sons. f) Schematic of the interlocked switching mechanism in the IP and OOP states (State 1 → State 2), where Se and In atoms are painted yellow and blue, respectively. g) Pinched hysteretic curves as the maximum V_{Drain} sweeps from 2 to 6 V. The arrows exhibit the sweeping orientations. h) Transfer characteristics of the gate-tunable α-In_2Se_3 memristor under the vertical electric field. i) Channel conductance switching under the ferroelectric polarization reversal, regulated by the gate bias. The read bias is implemented on the drain-source terminal. j) Output characteristics at distinct gate voltages. The positive gate voltages significantly suppress resistance switching, whereas the negative gate voltages facilitate its recovery. f-j) Reproduced with permission.[136] Copyright 2019, John Wiley and Sons. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.).

the positive V_{max} (sweep ii) and then is reset to 0 V (sweep iii). When the V_{Drain} is reduced below 0 V, the resistance state switches to the HRS (sweep iv). Thus, the sweeps from i to ii corresponding to LRS–HRS transitions can be worked as memristor, exhibiting a high switching ratio of 10^3 at $V_{max\text{-}sweep}$ above 4–5 V. Introducing a gate control for a two-terminal ferroelectric memristor, generally referred to as a ferroelectric memtransistor, is essential for fundamental research and device designs. Notable hysteresis transfer characteristics in Fig. 6h demonstrate the effective channel conductance regulation in the memtransistor and its corresponding ferroelectric polarization switching. As the vertical (or OOP) gate bias is above +35 or −35 V, the OOP ferroelectric polarization in the ferroelectric α-In_2Se_3 could be switched upward or downward. The channel resistance states of the memtransistor are later regulated to the LRS or HRS, corresponding to the left or right IP polarization. As the gate voltage is beyond ±40 V, some variations, probably owing to the screening effect on the polarization charge, can be observed, where the reverse-forward sweep at 0 V mutually gets close. The gate-write/drain-read performance in Fig. 6i exhibits that external gate bias can reverse the interlinked upward-leftward ferroelectric dipoles, which is almost normal for the planar device. These findings provide the first evidence that the switching of ferroelectric polarization in ferroelectric materials can be initiated by a gate bias and optimized through associated resistance switching (Fig. 6j). Benefiting from the ferroelectric semiconducting nature of the α-In_2Se_3 channel, the current switching ratio of the α-In_2Se_3 memtransistor can be adjusted from 0 to more than tenfold, corresponding to distinct channel polarization states by varying the gate bias. The memtransistor benefits from the ferroelectric semiconducting nature of the α-In_2Se_3 channel and demonstrates excellent performance tunability, such as channel conductance, ferroelectric polarization flipping, current switching ratio, etc., making it highly promising for future functional electronics.

Non-volatile memory

Ferroelectric-based memories, generally with stable polarization states,[138] are promising candidates for persistent data storage technologies owing to their electrically writable non-volatile states. Due to the poor interface quality and thermodynamic instability resulting from the unsaturated dangling bonds of the bulk ferroelectrics, 2D layered ferroelectric-based devices demonstrate greater advantages in retention endurance, and commercialization compared to conventional ferroelectric devices. Fig. 7a exhibits the schematic structure of the CIPS/WSe_2 FeFETs comprising a buried Ti/Au gate electrode, in which the CIPS serves as the gate insulator and WSe_2 works as the semiconductor layer, respectively. The transfer characteristics of the device exhibit a bipolar behavior with a clockwise hysteresis from bidirectional scanning (Fig. 7b). Considering that majority carriers in WSe_2 semiconductors are positively charged holes, the working principle of the FeFETs can be explained as follows. As a positive voltage above the coercive voltage is placed on the buried gate, the dipoles within the CIPS ferroelectric gate dielectric upwardly align towards WSe_2, causing a negative charge accumulation on the top surface of CIPS. These bound negative polarization charges attract positive holes from the WSe_2 channel to the interface region, which effectively screen the negative

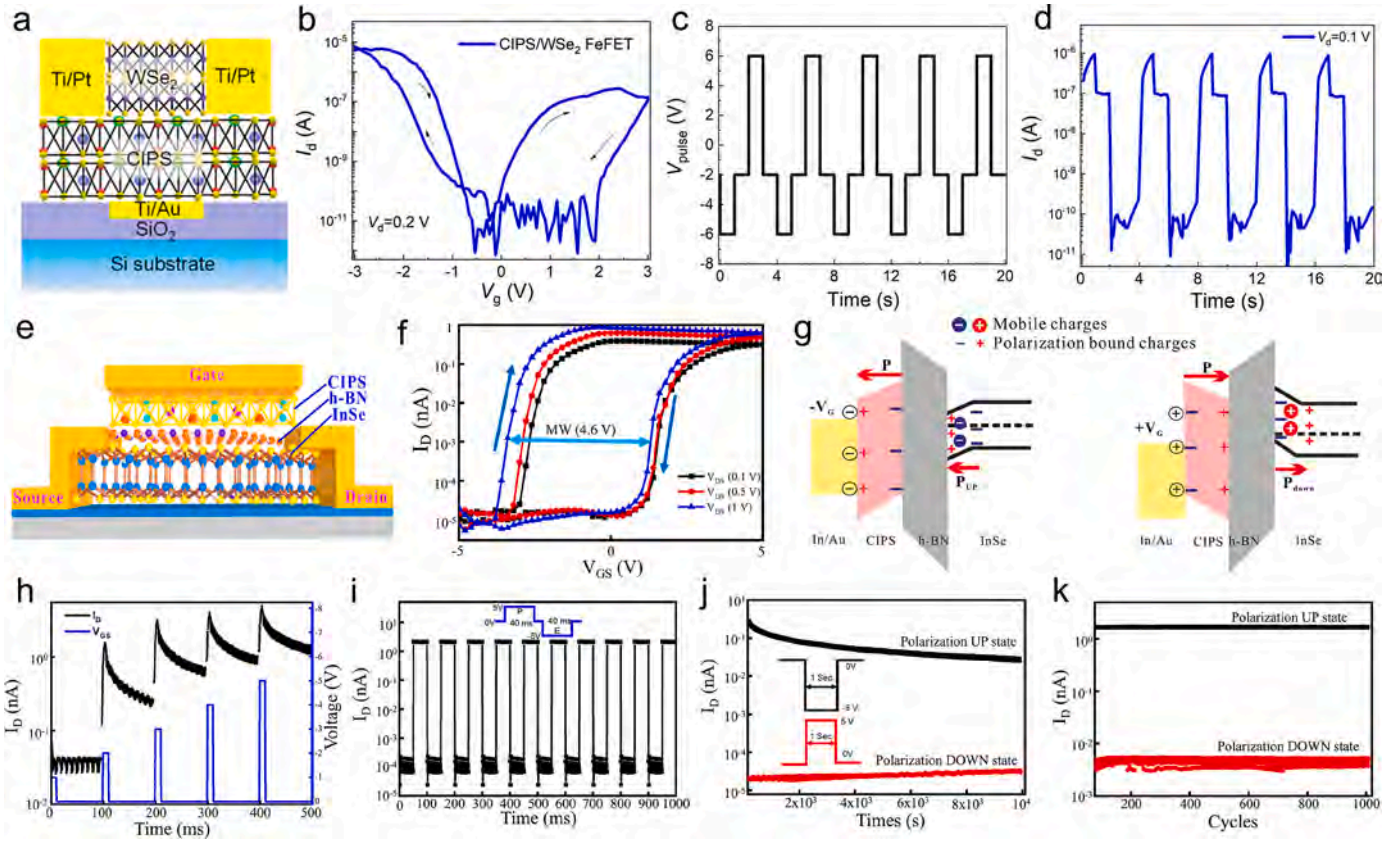


Fig. 7. a-b) Schematic illustration of the FeFET based on the WSe_2/CIPS heterostructures (a) and its corresponding transfer curves at V_d = 0.2 V (b), respectively. c-d) Input pulse bias (c) and related output current (d) of the WSe_2/CIPS FeFET under V_d = 0.1 V. a-d) Reproduced with permission.[146] Copyright 2021, American Chemical Society. e) Schematic of a 2D InSe vdWH FeFET, in which CIPS and h-BN function as the ferroelectric gate and insulating layers, respectively. f) Transfer curves of the 2D InSe vdWH FeFET at distinct V_{DS} in the bidirectional sweep mode. (g) Band diagrams of the CIPS/h-BN/InSe FeFET under opposite gate voltage exhibiting distinct types of charge accumulation. h) Output current response in response to the distinct input biases. i) Dynamic behavior of the FeFET in response to the periodic gate voltage. j-k) Performance test of the dynamic characteristics (j) and related program and erase endurance cycles (k), respectively. e-k) Reproduced with permission.[110] Copyright 2022, American Chemical Society.

polarization charges. Consequently, holes become localized owing to the accumulation of polarization charges, causing a depletion of holes and a reduced channel conductance in WSe_2.[139] In contrast, applying negative biases to the buried gate reverses the polarization orientations of dipoles in the CIPS ferroelectric gate dielectric towards WSe_2. This induces positive charges on the top surface of CIPS, attracting electrons from CIPS to the interface region. Thus, positive polarization charges are effectively screened, enhancing hole carrier density and conductance in WSe_2. Intriguingly, a clockwise hysteresis curve, instead of a typical counterclockwise hysteresis,[140,141] is also observed in the electron branch, which could be attributed to the electrons de-trapping from the acceptor-like traps in WSe_2.[142] To evaluate the reliability of the device in non-volatile memory applications, the output current changing with the pulse voltage at $V_{ds} = 0.1$ V is investigated. Fig. 7c demonstrates the experimental setup where the periodic pulse is applied with a fixed amplitude of 6 V and pulse width of 1 s. As depicted in Fig. 7d, it was observed that the programming (P) and erasing (E) states alternated periodically as the applied pulse varied accordingly.

Recently, Lee et al. developed a full-vdWs integrated metal-ferroelectric-insulator-semiconductor (MFIS) FET memory cell on a 285 nm SiO_2/Si substrate for non-volatile memory (NVM) applications. [110] Fig. 7e exhibits the schematic of the NVM device, in which the mechanically-exfoliated CIPS (~70 nm), h-BN (~8 nm), and InSe (~10 nm) serve as the top ferroelectric, insulating, and channel layer, respectively. The transfer characteristic of the top-gated vdW FeFET demonstrates a large hysteresis window (Fig. 7f), simultaneously with a high current on/off ratio of 10^4 and a subthreshold slope of 147 mV/dec. Moreover, the transfer curves demonstrate a clockwise hysteresis for an n-type semiconductor, distinct from the typical 2D vdWH Fe-FET.[100, 140,143] Attributing to the coexistence of polarization-bound charges and mobile charges in the InSe film, the mechanism of the InSe conductance is distinct from the conventional semiconductors due to its unique charge distribution. Fig. 7g shows the CIPS/h-BN/InSe FeFET schematic band diagrams under forward and reverse gate bias, respectively. Under negative gate voltages, InSe and CIPS flakes polarize up with positive-bounded charges at the top of the channel surface, accumulating the mobile electrons at the bottom surface to form an LRS of the channel. Due to the high-EOT CIPS/h-BN layers, the insufficiently strong electric field prevents complete polarization reversal across the whole InSe layers. Instead, only a partial polarization reversal, limited to a few InSe layers, can be induced. In the device, the InSe dipoles at the interface are robustly regulated by the polarized CIPS flakes under the external electric field. The coupled dipoles of the two ferroelectrics could lead to a stable charge density at the h-BN/InSe interface that ensures the channel resistance states of the InSe layer beyond the coercive voltage of CIPS. The transient response as the gate bias increases from −1 to −5 V is tested by a pulse train of 10 ms, exhibiting a continuous increase of the drain current (Fig. 7h). The result demonstrates that after a short-duration pulse, the ferroelectric polarization reversal can realize the LRS in the CIPS/h-BN/InSe device.

Fig. 7i exhibits the program/erase (P/E) states through the current dynamic response, in which a stable dynamic P/E ratio of above 10^3 without apparent degradation can be inspected at $V_{DS} = 1$ V. Key parameters, e.g., the retention and endurance characteristics are tested for benchmarking the performance and reliability of the device under a particular gate and drain bias. Fig. 7j shows a one-order magnitude of current degradation throughout the test duration, exhibiting a reliable channel conductance regulation during ferroelectric polarization. A train of the alternative pulses with magnitudes of ±5 V and a time interval of 50 ms are used to test the endurance, in which the related currents are read with a source/drain bias of 100 mV. There are almost no current changes after 10^3 test cycles, and the on/off current ratio can remain $>10^3$ under up and down states (Fig. 7k). Compared with the 3D ferroelectrics, the dangling-bond-free vdWs CIPS/h-BN/InSe heterostructures intrinsically with smaller inter-gaps shows more effective channel regulation by ferroelectric field as the dipole electric field is proportional to R^{-3} (R, surface-to-depth distance).[144,145] The device's strong durability and persistence features are owing to the synergistic effect of ferroelectric CIPS and InSe in the vdW heterostructures, which is consistent with the test result of the TEM, PFM, and electrical measurements.

Artificial synapse

Considering the rapid computational speed and high energy efficiency of the neuromorphic systems, the emulation of neural functions of the human brain is viewed as a potential strategy for next-generation computing.[147] The mimicry of biological neurons by artificial synapses and neurons in the neuromorphic systems is highly required since information needs to be gone through the interlinked neurons to the nervous system.[148] To implement an artificial synapse, the response of biological neurons needs to be emulated by replacing the synaptic weight with the variation of the conductance (resistance).[149] The artificial synapse exhibits two types of synaptic plasticity, namely long-term plasticity (LTP) and short-term plasticity (STP),[150] relying on the persistence of the memory. Currently, brain-like computing hardware based on the units of the Fe-FETs has been revealed as a front-runner for developing future artificial neural hardware.[151] However, neuromorphic synaptic devices based on bulk materials inevitably face dangling-bonds-induced defects and impurities as device dimension scales down, limiting their stability and functionality. In contrast, 2D ferroelectric-based devices without unpaired bonds surface in ferroelectric layers are qualified with better tolerance against performance degradation and functionality.

Lee et al. present an all-ferroelectric Fe-FETs that utilizes 2D ferroelectrics in both the gate insulator and channel layers,[152] which are the active components of the FET structure. Fig. 8a schematically demonstrates the synaptic device that can emulate the dynamics of a biological synapse, where the flakes in the device are mechanically exfoliated and sequentially transferred onto the SiO_2/Si substrate with a per-layer thickness of α-In_2Se_3 (52 nm), h-BN (6 nm), and CIPS (84 nm), respectively. Both FeSFET (α-In_2Se_3/h-BN) and vdWH FeFET (α-In_2Se_3/h-BN/CIPS) show an n-type behavior with clockwise hysteresis, but the latter shows a much larger memory window than the FeSFET (Fig. 8b). This result can be attributed to the ferroelectric polarization of CIPS that improves the channel conduction of the α-In_2Se_3 ferroelectric semiconductor. As shown in Fig. 8c, the energy band diagrams of the α-In_2Se_3/h-BN/CIPS heterostructure in polarization up and polarization down states illustrate its working mechanism. Compared to the 2D ferroelectric CIPS that merely has polarization-bound charges, ferroelectric semiconductors (α-In_2Se_3) have mobile and polarization-bound charges owing to the coupling of the semiconducting and ferroelectric characteristics. Considering the relatively high EOT of the gate dielectric layers, only partial ferroelectric polarization reversal can be induced in the α-In_2Se_3 channel as the gate voltages sweep. The polarization-bound charges in the CIPS and α-In_2Se_3 layers align in a polarization up state under a negative gate bias, while a positive gate bias aligns them in a polarization down state. Therefore, the downward (upward) band bending and channel accumulation (depletion) at the top surface of α-In_2Se_3 arise, leading to a low (high) resistance state. The working mechanism results in clockwise hysteresis. The interlayer coupling of the polarization-bound charges in the CIPS and In_2Se_3 layer facilitates the coupling of their dipoles in one direction by an electric field, maintaining the polarization states and achieving larger memory windows. It is depicted that the ratio of the memory window (M.W.) to sweep range (S.R.) shows a linear increase as the V_{GS} sweep ranges rise, reaching a maximum M.W./S.R. ratio of 72 % for a memory window of 14.47 V at a V_{GS} of 10 V. By utilizing the electrical stimulation at the weight control terminal (WCT), partial ferroelectric switching appears, producing either potentiation or depression of the channel conductivity.[153] To check the traits of excitatory/inhibitory postsynaptic currents (EPSCs and IPSCs) stimulated by V_{wc} pulses, the

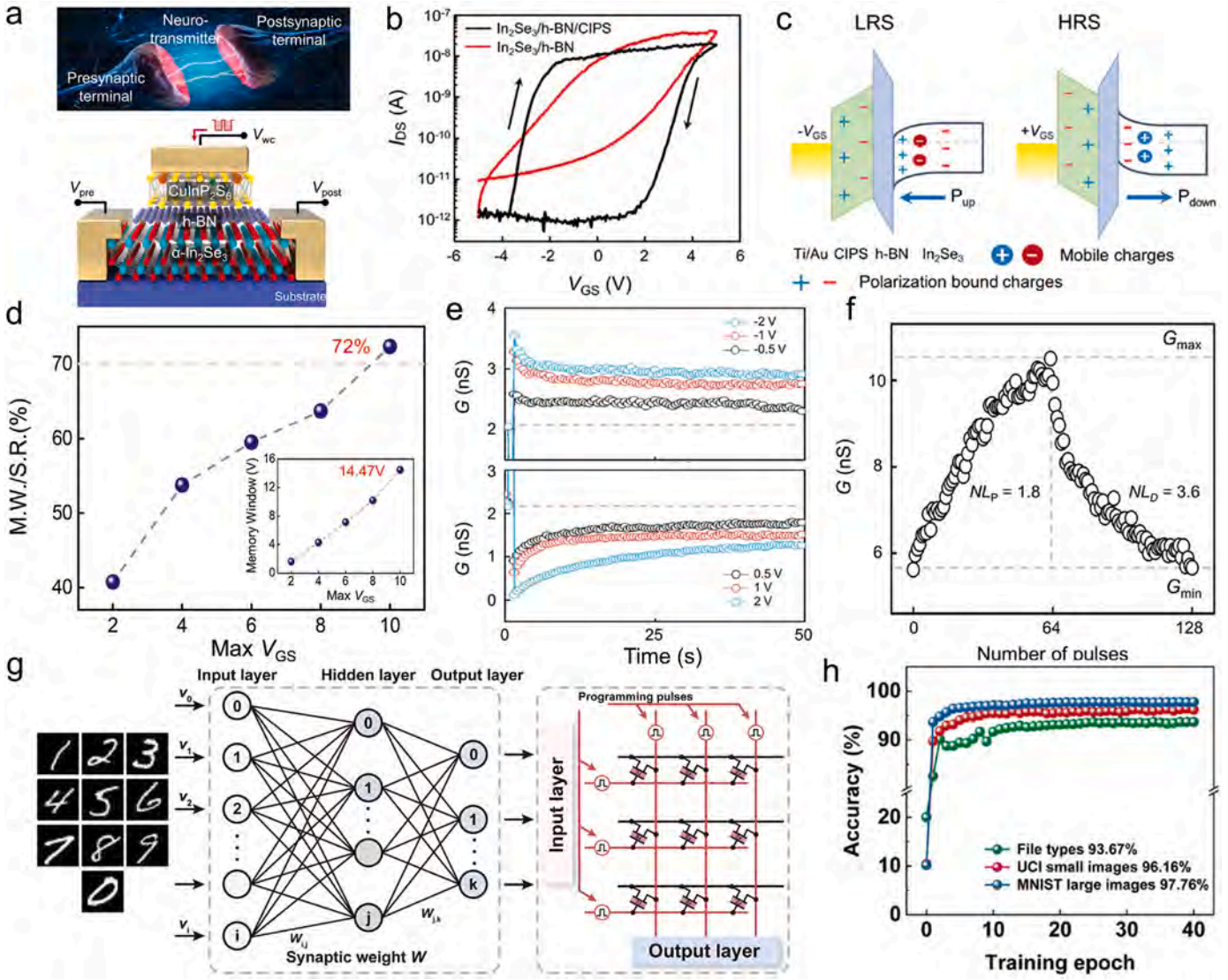


Fig. 8. a) Schematic demonstration of the biological synapse and three-terminal vdWH α-In_2Se_3/h-BN/CIPS Fe-FET synapse device. b) Comparison of transfer characteristics between the α-In_2Se_3/h-BN/CIPS (black) and α-In_2Se_3/h-BN (red) FeFETs at a fixed V_{DS} = 1 V as the gate bias sweeps from −5 to +5 V. c) Band diagrams of the α-In_2Se_3/h-BN/CIPS Fe-FET device under polarization up (left) and down (right) state, respectively. d) M.W./S.R. ratios increase with the max V_{GS}. Inset demonstrates that the memory window linearly increases with the max V_{GS}. e) Excitatory (upper) and inhibitory (lower) postsynaptic conductance responses (EPSC/IPSC) in response to the electrical pulse imposed on the weight control terminal (WCT). f) Conductance changes of the LTP/LTD features based on the number of pulses with NL of 1.8 and 3.6. a-f) Reproduced with permission.[155] Copyright 2022, John Wiley and Sons. g) Schematic of the neural networks comprising input neurons, hidden neurons, and output neurons (middle), along with the correlated synaptic circuits of the conceptual neural networks (right). h) Accuracies of the ANNs with the artificial synapse after 40 training epochs for the file type, the UCI, and the MNIST datasets, respectively. g-h) Reproduced with permission.[154] Copyright 2022, John Wiley and Sons.

V_{wc} pulses with varying amplitudes (±0.5 to ±2 V) and a constant time interval (100 ms) to the WCT are applied to measure the conductance ($G = I_{psc}/V_{post}$) by adopting a fixed V_{post} of 1 V (Fig. 8e). For EPSCs, the conductance gradually rises as Vwc pulses increase and drops accordingly as the identical Vwc pulses decrease for IPSCs. In either case, the conductance does not restore to the initial condition at a time interval of 50 s after applying the Vwc pulses. To examine the effects of Vwc pulses on long-term potentiation/depression (LTP/LTD) characteristics, the 64 excitatory/ 64 inhibitory V_{wc} pulses are applied by measuring the changes in conductance (Fig. 8f). Under consecutive 64 excitatory/ 64 inhibitory V_{wc} pulses, the channel conductance potentiated from 10.0 to 22.6 nS with the nonlinearity (NL) of 1.8 and depressed from 22.6 to 9.31 nS with the NL of 3.6, respectively. This result indicates that the dipoles of the CIPS and *α*-In_2Se_3 are gradually reversed by the induced E-field, leading to a gradual conductance change under applying sequential electrical pulses.

To demonstrate the implementation of the ferroelectric semiconductor (FES) synapses in the neural network via back-propagation (BP) algorithms, a three-layer artificial neural network (ANN) was trained by the Sandia file types data set, the UCI (8 × 8 pixels) data set, and the MNIST (28 × 28 pixels) handwritten digits data set (Fig. 8g).[154] The voltage signals (V_i) associated with individual pixels within the patterns across diverse datasets were applied to the input neuron layer. Followed by multiplying synaptic weight ($W_{i,j}$), the weight sum currents ($I_i = \sum_{i=1}^{i} W_{i,j} \times V_i$) can be transformed for the *j-th* current in hidden layer.[154] Subsequently, the hidden voltage signals are calculated using the sigmoid activation function and experienced analogous operations across the two layers. Subsequently, the output value k was compared with each labeled value to evaluate the error. The synaptic weights were renewed by optimizing the errors utilizing the BP algorithm. The synaptic weight was preassigned as the conductance values of

the α-In_2Se_3 memtransistor-based synapse ($W = G$), and all neurons in a sublayer have full connectivity with all neurons in the next layer via an electronic synapse. After 40 training epochs, the ANNs using the artificial synapse showed notable accuracies of 93.67 %, 96.16 %, and 97.76 % for the file type, UCI, and MNIST datasets, respectively. Owing to the switchable ferroelectric polarization reversal in α-In_2Se_3, the neural networks based on the α-In_2Se_3 memtransistors exhibit significant advantages in achieving characteristics of configurable near-ideal linearity and symmetry, multilevel conductance states, and small conductance response variability. These results exhibit the potential of the 2D vdWH ferroelectrics in Fe-FET as a forerunner in exploring prospective artificial synaptic applications.

NC-FET inverter

Data-center-driven epoch is ushering in a transformative new paradigm with prospects in all sectors, particularly for silicon-based electronics, in which power consumption is growing into a core concern for electronic circuits.[156] It can be attributed that the supply voltage scaling could not catch up with the reduction of the typical dimension of conventional transistors due to the physical constraint known as "Boltzmann Tyranny," which indicates that a minimal gate voltage of 60 mV is needed to regulate the drain current by one order of magnitude.[157] To address this concern, numerous innovative transistor architectures have been devised to reduce the subthreshold swing (SS) below the theoretical limit with decreased supply voltage and power consumption.[158–160] As an emerging FET architecture, negative capacitance FET (NC-FET) can potentially overcome Boltzmann's limit for traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) in building ultra-low-power-consuming electronics.[161] This is because the NC-FETs can promisingly overcome the thermionic-limit subthreshold slope (SS) of 60 mV dec^{-1} at room temperature by utilizing ferroelectric materials to amplify the gate voltage internally. Due to the atomically thin features of 2D ferroelectric materials, 2D ferroelectric-based NC-FETs are relatively exempted from short-channel-effects and suitable for achieving steep SS values below 60 mV dec^{-1}.[162] At present, though NC-FETs using traditional thin-film ferroelectrics, e.g., ferroelectric hafnium zirconium oxide (HZO)[163] or polymer[164], etc., as the ferroelectric gate has been explored, the research on 2D ferroelectric-based NC-FETs is still on its

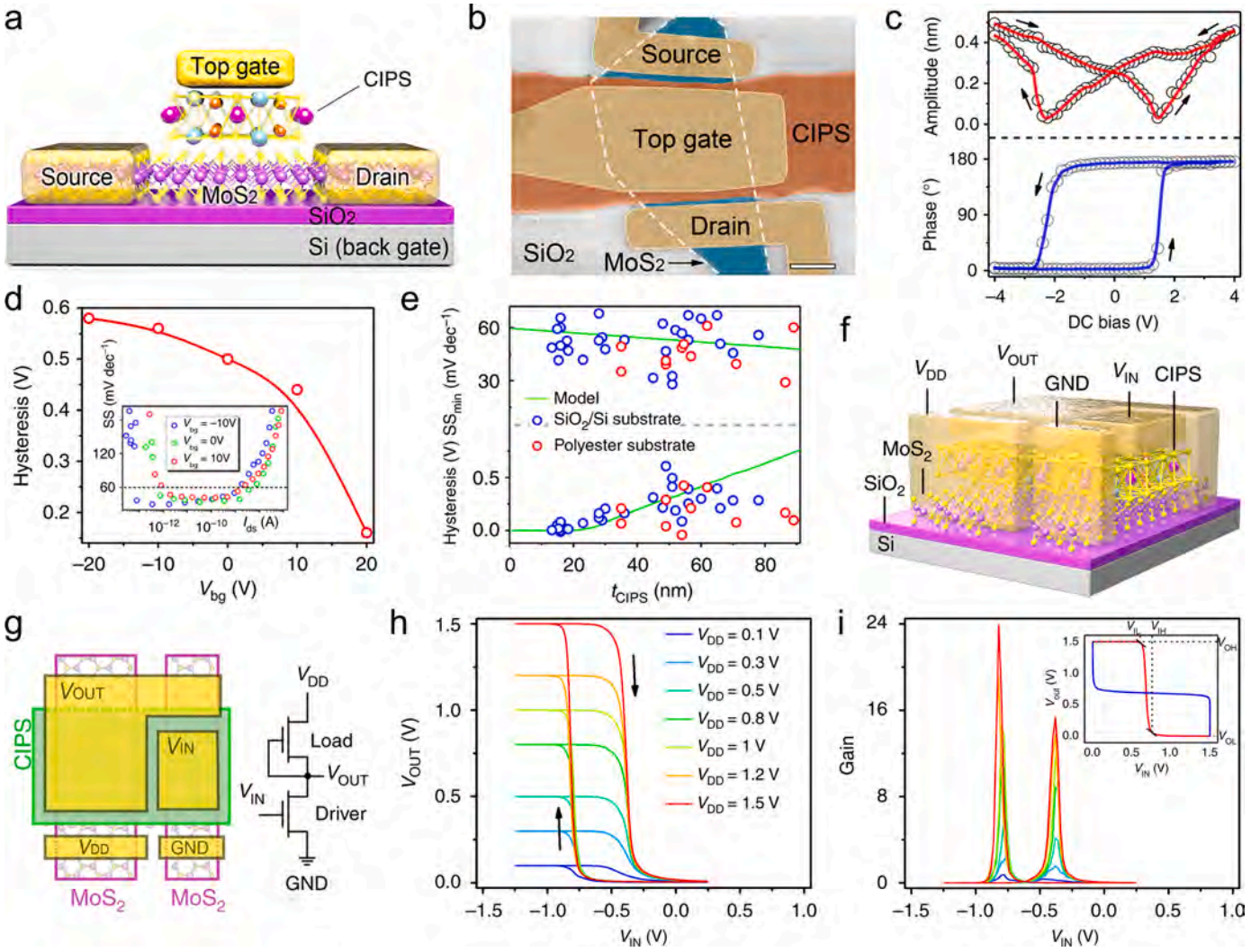


Fig. 9. a-b) Schematic illustration of the CIPS/MoS_2 vdW NC-FET (a) and corresponding SEM image of the device (b) with a scale bar of 2 μm. c) Hysteresis curves of the "OFF-field" amplitude (upper) and phase (lower) test for CIPS during the reversal process. d) Hysteresis dependence on the V_{BG}. The Inset image demonstrates the extracted SS for distinct gate voltages (V_{BG}). e) SS (top) and hysteresis width (bottom) dependence on CIPS thickness, where symbol and line represent experimental and simulated data, respectively. f-g) Schematic illustration of the device structures (f) and circuit of the vdW NC-FET inverter (g). h) V_{OUT}-V_{IN} characteristics of the logic inverter at different V_{DD} from 0.1 V to 1.5 V. i) Voltage gain of the NC-FET inverter at distinct V_{DD}. The Inset image shows the noise margins of the inverter at V_{DD} = 1.5 V. Reproduced with permission.[170] Copyright 2019, Springer Nature.

infancy. Due to the advantages of the atomically smooth surface in optimizing the interface traps,[165] the 2D ferroelectric-based NC-FETs would possess excellent performance since the NC effect shows a strong correlation with the ferroelectric domain flipping at the interface.

Fig. 9a shows the device structure of a CIPS/MoS_2 vdW NC-FET structure, in which the MoS_2, CIPS, and SiO_2 layer separately function as semiconductor channel, ferroelectric and gate insulator.[166] As shown in Fig. 9b, the false-colored image displays the top view of the device configuration. The off-field PFM test under dual AC resonance tracking (DART) mode exhibits the amplitude and phase hysteresis curves during the reversal process, where a butterfly curve and clear 180° phase reversal are observed (Fig. 9c), confirming the ferroelectricity of CIPS flakes.[47] The top-gate transfer characteristics of NC-FET are examined by applying the back-gate bias, demonstrating effective suppression for the ferroelectric hysteresis and slight enhancement of the SS under positive and negative V_{bg}, respectively (Fig. 9d). This result could be attributed to the effective regulation of CIPS capacitance (C_{CIPS}) under gate bias since the NC-FET can be viewed as a primary 2D FET integrated with a ferroelectric CIPS capacitor.[94,166] Thus, the amplification gain of the internal gate voltage, denoted as A_V, can be calculated as $A_V = |C_{CIPS}|/(|C_{CIPS}| - C_{int})$, where C_{int} represents the top-gate capacitance of the device. Therefore, the SS can be derived as $SS_{NCFET} = SS_{2DFET}/A_V$. To acquire a small SS and large A_V, C_{int} should be close to $|C_{CIPS}|$, whereas C_{int} should be beneath $|C_{CIPS}|$ to avoid hysteresis. Increasing the channel charges under applying a positive V_{bg} could produce a larger $|C_{CIPS}|$, causing a decreased hysteresis and an enhanced SS for NC-FET.

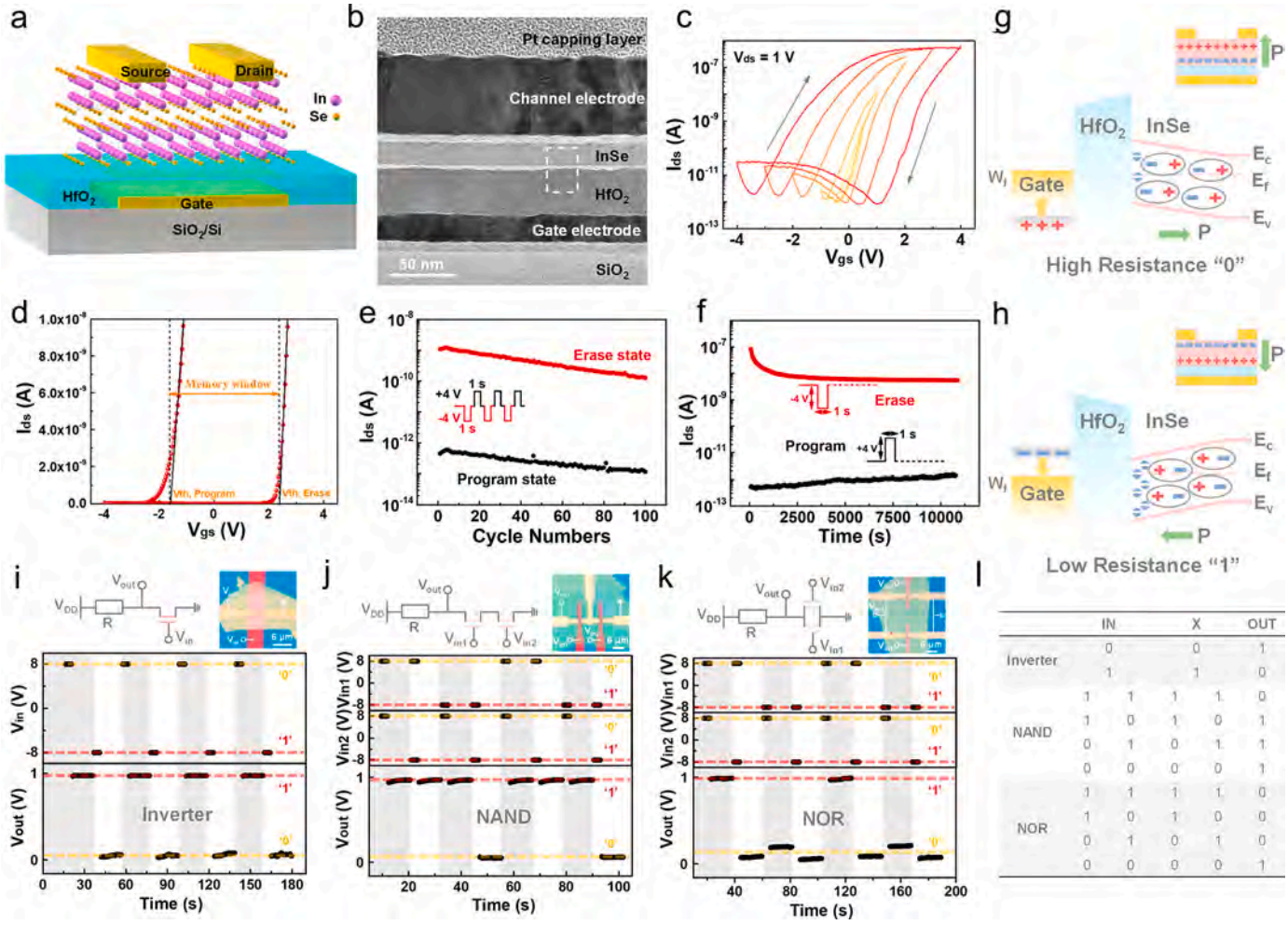
Besides, as the CIPS thicknesses decrease, the $|C_{CIPS}|$ rises with a slight gate-voltage amplification A_V and reaches the non-hysteretic situation (($|C_{CIPS}| > C_{int}$). Fig. 9e shows the dependence of SS and hysteresis on CIPS thickness, and 28 NC-FETs with different CIPS thicknesses changing from 13 to 80 nm are summarized, among which the majority (21 devices) presents ultralow SS below 60 mV dec^{-1} at room temperature. Based on the high-performance NC-FETs, the logic inverters are prepared to reveal the possibility of designing low-power devices. Fig. 9f-g exhibits the device structure of the related logic inverter with two interconnected CIPS/MoS_2 vdW NC-FETs, acting as the separate pull-up load ($W/L = 5.4/4.0$) and pull-down driver ($W/L = 2.4/5.5$) accordingly. As shown in Fig. 9h, the voltage transfer characteristics of the inverter, plot of input (V_{IN}) versus output voltage (V_{OUT}), under different supply voltages (V_{DD}) are investigated. Regardless of the forward and backward sweeps, signal inversions occur with high V_{OUT} at low $V_{IN,}$ even down to 0.1 V. As demonstrated by Fig. 9i, a maximum voltage gain of ~24 could be reached for $V_{DD} = 1.5$ V, relatively higher or comparable with TMDs-based MOS inverters.[167,168] The high-gain inverter based on 2D ferroelectric NC-FETs combines ferroelectric materials science and device engineering, laying the foundation for designing low-power and ‘‘steep-slope’’ device architecture.[169]

In-memory computing

In the Internet of Things (IoT) and Artificial Intelligence (AI) age, the proliferation of data-intensive applications has led to considerable data transfer between processors and memories. Nevertheless, the bandwidth restriction of the Von Neuman architecture between processors and memories unavoidably degrades system efficiency and power conservation, referred to as a memory wall.[171] In-memory computing offers a highly-efficient way to break the bottlenecks of von Neumann architectures in minimizing redundant latency and energy expenditure during massive data transfer processes since conventional memory and processing units are separated by geography. To overcome the problem of memory walls, enormous device designs, particularly for in-memory computing architecture, have been demonstrated,[172–175] in which the device architectures generally adopt a floating gate to provide both charge-trapping and field-modulating units. Different from the floating-gated charge-trapping mechanism in conventional structure, 2D ferroelectric-based architectures for in-memory computing generally work based on ferroelectric order parameters to regulate the channel conductivity. Under external electric stimuli, most prominent merits of 2D ferroelectric devices relying on ferroelectric order parameters could principally possess fast response speed and high reliability.

Very recently, Xie et al. have developed a metal-oxide-ferroelectric semiconductor transistor (MOfeS-FET) for in-memory computing, where the vdWs ferroelectric semiconductor (InSe) and HfO_2 function as channel material and dielectric insulator, respectively (Fig. 10a).[176] High-resolution scanning transmission electron microscopy imaging in Fig. 10b exhibits a sharp boundary interface with even thicknesses, demonstrating the nonexistence of interface diffusion and destruction in the device structure. Moreover, atomically thin 2D InSe could polarize within the device, potentially suitable for integrating the memory and logic capabilities in the same materials.[100,177] The OOP ferroelectric polarization in InSe is proper for data storage, while its semiconducting property is applicable for logic computation. The transfer characteristics under bidirectional V_{gs} sweeps exhibit an n-type semiconducting property (on/off ratio of 10^6) with clockwise hysteresis windows for the 2D MOfeS-FET (Fig. 10c). The forward and backward transfer curves shift to the opposite directions as the range of the V_{gs} increases, e.g., the memory window raises to 3.9 V at $V_{gs} = 4$ V (corresponding to two distinct OOP ferroelectric polarizations in InSe) (Fig. 10d). Fig. 10e exhibits the fatigue-free P/E characteristics of the device between LRS and HRS under the gate program/erase pulses above 100 cycles. The device structure also presents excellent retention characteristics at both programs (10^{-13}–10^{-12} A) and erase states (10^{-8}–10^{-9} A) after the V_{gs} pulse (Fig. 10f). The band diagrams of the metal-HfO_2-InSe heterostructure under upward and downward polarization are demonstrated (Fig. 10g-h), in which electrons and polarization-bounded charges exist in the InSe channel due to the coupling of the semiconducting and ferroelectric characteristics.[100,110] The energy band bends up under a positive gate bias that exceeds the coercive voltage, leading to an aligned polarization against the HfO_2/InSe interface (Fig. 10g). Therefore, within the InSe channel, the electrons (charge carriers) deplete, leading to an HRS. If a negative gate bias (higher than the coercive basis) is utilized, the polarization orientation will align towards the HfO_2/InSe interface (Fig. 10h). The mobile electrons accumulate, resulting in an LRS. The band diagram analysis is consistent with the dynamic characteristics of the MOfeS-FETs, namely the resistance switching between the program and erase states by regulating the alternating positive and negative gate bias.

Further, the in-memory computing based on the InSe MOfeS-FET with a bias resistor in series is exhibited, in which the input positive and negative V_{gs} bias represent a logic “0″ (“1″), respectively. The input signal corresponding to the device state can be regulated and maintained as memory logic state X. Fig. 10i presents the schematic of a programmable inverter integrated with a 10 GΩ resistor and its performance for logic computation under ±8 V gate pulses. After applying the positive pulse (+8 V), the device can be set to the HRS (input logic “0″) and well maintained in the channel. The output voltage at the junction of the MOfeS-FET and the serial resistance was about 1 V (logic “1″). Conversely, the negative Vgs pulse (−8 V, input logic “1″) can program the device to the LRS, corresponding to the output voltage of about 0 V (logic “0″). These results demonstrate the realization of logic inversion and final result storage. More importantly, NAND and NOR’s more sophisticated Boolean logic operations have been constructed in conjugated MOfeS-FET circuits (Fig. 10j-k). In the device configuration of the NAND and NOR circuits, two bottom electrodes function as two input terminals (IN1 and IN2), while the output voltages of the circuit are still referred to as the logic output signal. As a voltage pulse of +8 V is applied to two metal gates (IN-00), both devices are switched to the HRS. The output voltage was around 1 V at a V_{DD} of 1 V, referred to as a logic "1″. The processing outcome of IN-00 was stored in situ by the memory and processing system. Similarly, a high output voltage (logic “1″) could be generated and reserved, while a low output voltage of 0 V



	IN		X	OUT
Inverter	0		0	1
	1		1	0
NAND	1	1	1	0
	1	0	1	0
	0	1	0	1
	0	0	0	1
NOR	1	1	1	0
	1	0	1	0
	0	1	0	0
	0	0	0	1

Fig. 10. a-b) Schematic demonstration (a) and cross-sectional test (b) of the 2D InSe MOfeS-FET. c) Transfer characteristics of the device under different bidirectional gate sweeps. The clockwise hysteresis enlarges with the increase of the Vgs, suggesting the sequential enhancements of the OOP ferroelectric polarization. d) Transfer characteristics of the device in the program and erase states, in which the memory window refers to the threshold voltage (V_{th}) difference between the program and erase states. e-f) Dynamic performance under 100-cycle alternate erase (−4 V, 1 s) and program (4 V, 1 s) test (e), and retention characteristics of the device (f). The current is read at $V_{ds} = V_{gs} = 1$ V. g-h) Schematic band diagrams of Metal/HfO_2/InSe heterostructures under two opposed ferroelectric polarization orientations, HRS (g) and LRS (h) state, respectively. i-k) Schematic illustration of the programmable circuit and function for logic computation, including inverter (i), NAND logic operation (j), and NOR (k), respectively. l) Corresponding truth table of the inverter, NAND, and NOR logic. All the output voltages were observed at $V_{DD} = 1$ V and $V_{gs} = 3$ V. Each resistor applied in the inverter and NAND/NOR is 10 GΩ. Reproduced with permission.[178] Copyright 2023, American Chemical Society.

(logic "0″) is obtained for IN-11 (Vin1 = Vin2 = −8 V). A shunt-wound device structure was further adopted to investigate the performance of the NOR operation (Fig. 10k). At a negative gate pulse (IN-11, IN-10, and IN-01), the devices are programmed to the LRS, corresponding to the output signals (logic "0″). The circuits with two input signals of logic "0″ (Vin1 = Vin2 = 8 V) are in the HRS, which corresponds to the output of logic "1″. The truth table (Fig. 10l) for the abovementioned inverter, NAND, and NOR circuits has demonstrated great potential in basic logical and non-volatile operations that can reduce transistors and promote the area efficiency for in-memory computing systems.

Summary and outlook

As the semiconductor industry develops rapidly, conventional 3D ferroelectric materials have been extensively explored in various engineering technology fields. However, these traditional ferroelectrics often encounter issues such as dielectric/ferroelectric instability or disappearance when their thicknesses scale below a critical value. Consequently, their miniaturization for industrial applications is limited by fundamental physical constraints. To address this limitation, the research focus has shifted towards the development of 2D ferroelectrics with atomically thin properties and easy integration capabilities. Although numerous 2D materials have been theoretically predicted and experimentally investigated to date, the study of 2D ferroelectrics is still in its early stages, with many challenges in ferroelectric physics yet to be overcome. 2D layered ferroelectrics have introduced a new paradigm to the science of ferroelectrics, in which stable monolayer and few-layer samples offer an excellent platform for examining the effects of reduced lattice dimensionality on long-range ferroelectric ordering. There remain numerous 2D ferroelectric systems with novel polarization mechanisms (such as sliding, charge-redistribution-induced, spin-driven, etc.), distinctive characteristics (such as negative piezoelectric coefficients and ferroelectric metallicity), and other unique ferroelectric physics to be uncovered. Through ongoing and dedicated research endeavors, significant progress has been made in understanding the underlying mechanisms of 2D ferroelectrics, accurately quantifying their properties, and successfully implementing them in a broad range of applications in ferroelectronics.

At the material level, effective techniques for finding 2D ferroelectrics with a suitable coercive field and remnant polarization, essential for ensuring device reliability, are still absent. Theoretical prediction is a useful indicator of our knowledge and, ideally, can direct experimental

choices. The development of precise prediction systems will consider the entire theoretical toolbox of computational materials science, which is broadly covered from machine-learning based force fields and first-principles molecular dynamics (MD) to methods of Monte Carlo (MC) and density functional theory (DFT) with various advanced features. These prediction methods will successfully find a large pool of 2D ferroelectric candidates with the appropriate electronic structure, such as effective mass, band degeneracy, Fermi velocity, etc., while simultaneously requiring less money and time than experimental studies. However, experimentally determining their spontaneous polarization is challenging due to the complex influence of factors such as strain, defects, dopants, and oxygen vacancies. To gain fresh insight into 2D ferroelectrics, cutting-edge characterization technologies are essential. For example, angle-resolved photoemission spectroscopy (ARPES) and scanning tunneling microscopy (STM) must work together to thoroughly map out the band structures of 2D ferroelectrics. More importantly, special test systems are crucial for 2D ferroelectric materials, such as a ferroelectric analyzer for P-E hysteresis loops, a second harmonic generator (SHG) for structure distortion, a dual AC resonance tracking PFM (DART-PFM) for ferroelectric order, etc., in contrast to the characterization techniques (such as X-ray diffraction, Raman, X-ray photoelectron spectroscopy, etc). Thus, developing strategies for studying 2D ferroelectrics, e.g., predication, characterization methods, etc., is of great necessity, which could lead to intriguing technological advances. Besides, most 2D ferroelectrics reported so far are still challenging to synthesize on a large scale regardless of directly synthesizing desired heterostructures, limiting their large-area device fabrication and high-density integration.

Though emerging 2D ferroelectric materials have been discovered, their compatibilities with 2D device fabrication and the CMOS process have not been sufficiently explored in contrast to conventional ferroelectrics. Given the rapid development of 2D electronics at the device level, there is a high demand for developing minimized and integrated functional electronics based on 2D ferroelectrics, which could launch a new scientific era of 2D ferroelectronics. However, current efforts mostly focus on individual devices, while integrating multiple devices into a functional system is still in its early stages due to the challenges associated with the mass production of highly reproducible devices. Additionally, there is a pressing need for scalable assembly techniques of 2D heterostructures that are compatible with existing complementary metal-oxide-semiconductor (CMOS) technology. Besides, considering the potential applications of 2D ferroelectrics, e.g., neuromorphic computing or artificial synapse, the strategies to achieve multiple polarization or resistance states in 2D ferroelectric materials need to be explored. At the materials level, the strategies, including strain engineering, interface engineering, thickness control, chemical substitution, etc., could be considered to regulate the crystal structure and polarization response, thus obtaining multiple polarization or resistance states of 2D ferroelectrics. Additionally, innovations in the device configurations, e.g., by adopting dual-gate FET, introducing tunneling layers, combining conventional ferroelectric layers, etc., are also promising directions to manipulate the multiple polarization states of 2D ferroelectrics. To sum up, more effective strategies are yet to be developed to obtain the multiple polarization states of 2D ferroelectrics.

In conclusion, research on 2D ferroelectronics is currently at an early stage. Numerous novel properties and diverse underlying mechanisms in 2D ferroelectrics are yet to be thoroughly explored. Successful exploration in this field necessitates interdisciplinary collaboration across various fields, including physics, chemistry, mechanics, engineering, materials science, and mathematics. To make significant progress in exploring 2D ferroelectrics, research studies across all these areas should be conducted simultaneously.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors do not have permission to share data.

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Supplementary materials

Supplementary material associated with this article can be found, in the online version, at doi:10.1016/j.mtelec.2023.100080.

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